

## N-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)
40	0.0088 at V <sub>GS</sub> = 10 V	50	16 nC
	0.0105 at V <sub>GS</sub> = 4.5 V	50	

### FEATURES

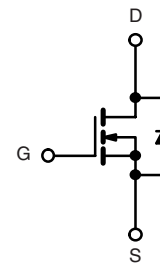
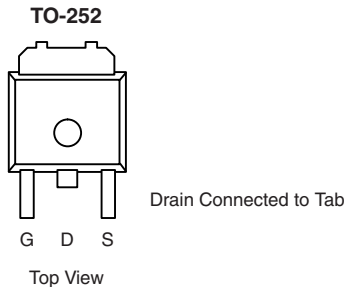
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Power MOSFET
- 100 % UIS Tested
- 100 % R<sub>g</sub> Tested
- PWM Optimized
- Compliant to RoHS Directive 2002/95/EC



RoHS  
COMPLIANT  
HALOGEN  
FREE

### APPLICATIONS

- LCD Display Backlight Inverters
- DC/DC Converters



Ordering Information: SUD50N04-8m8P-4GE3 (Lead (Pb)-free and Halogen-free)

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	40	V	
Gate-Source Voltage	V <sub>GS</sub>	± 20		
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	50 <sup>a</sup>	A
		T <sub>C</sub> = 70 °C	44	
		T <sub>A</sub> = 25 °C	14 <sup>b</sup>	
		T <sub>A</sub> = 70 °C	11.2 <sup>b</sup>	
Pulsed Drain Current	I <sub>DM</sub>	100		
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	40	
		T <sub>A</sub> = 25 °C	2.6 <sup>b</sup>	
Single Pulse Avalanche Current	I <sub>AS</sub>	30		
Avalanche Energy	E <sub>AS</sub>	45	mJ	
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	48.1	W
		T <sub>C</sub> = 70 °C	30.8	
		T <sub>A</sub> = 25 °C	3.1 <sup>b</sup>	
		T <sub>A</sub> = 70 °C	2.0 <sup>b</sup>	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>b</sup>	R <sub>thJA</sub>	32	40		°C/W
Maximum Junction-to-Case					

Notes:

a. Package limited.

b. Surface mounted on 1" x 1" FR4 board.

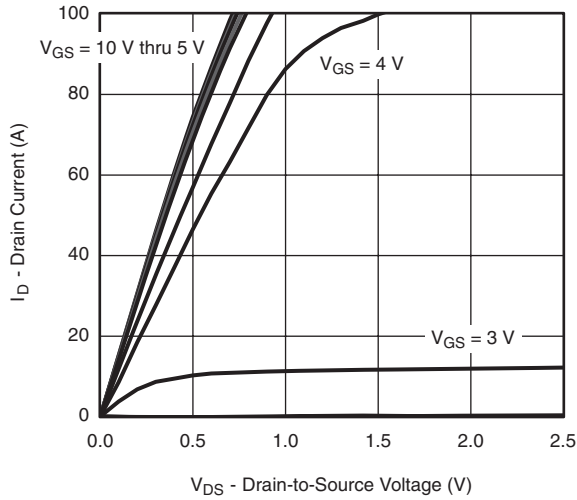
<b>SPECIFICATIONS</b> $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	40			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 1.0\text{ mA}$		44		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 5.9		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.5		3.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, T_J = 70\text{ }^\circ\text{C}$			20	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	50			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		0.0069	0.0088	$\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 15\text{ A}$		0.0084	0.0105	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 15\text{ A}$		75		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		2400		pF
Output Capacitance	$C_{oss}$			260		
Reverse Transfer Capacitance	$C_{rss}$			100		
Total Gate Charge	$Q_g$	$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		37	56	nC
				16	24	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 20\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$		6.5		
Gate-Drain Charge	$Q_{gd}$			4.5		
Gate Resistance	$R_g$	$f = 1\text{ MHz}$	2.5	5.5	8.5	$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 1\text{ }\Omega$ $I_D \cong 20\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		30	45	ns
Rise Time	$t_r$			15	25	
Turn-Off Delay Time	$t_{d(off)}$			45	70	
Fall Time	$t_f$			15	25	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 1\text{ }\Omega$ $I_D \cong 20\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		9	15	
Rise Time	$t_r$			5	10	
Turn-Off Delay Time	$t_{d(off)}$			40	60	
Fall Time	$t_f$			5	10	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$			40	A
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$				100	
Body Diode Voltage	$V_{SD}$	$I_S = 10\text{ A}$		0.81	1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 20\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		22	35	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			14	25	nC
Reverse Recovery Fall Time	$t_a$			11		ns
Reverse Recovery Rise Time	$t_b$			11		

Notes:

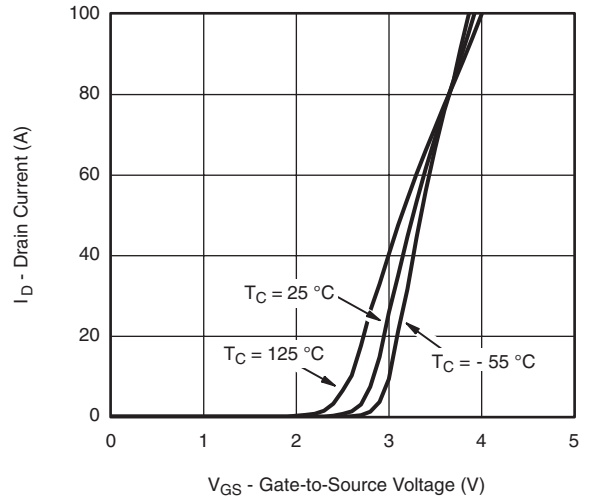
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

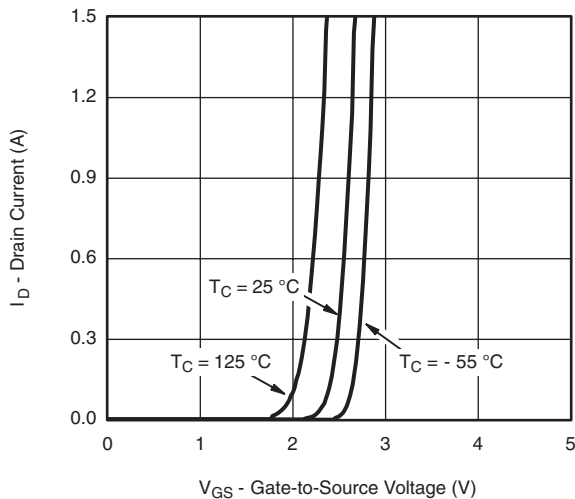
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



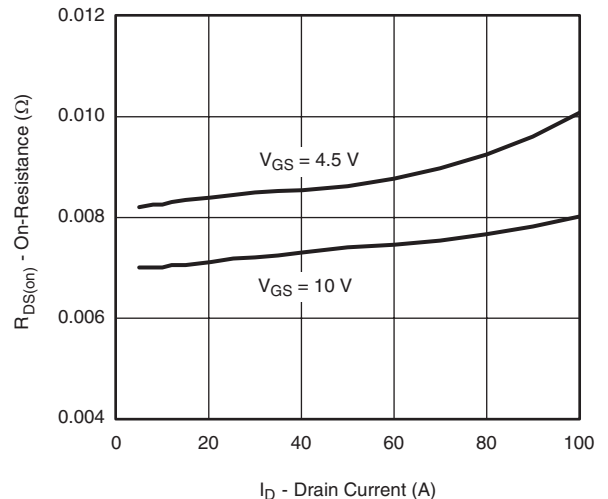
**Output Characteristics**



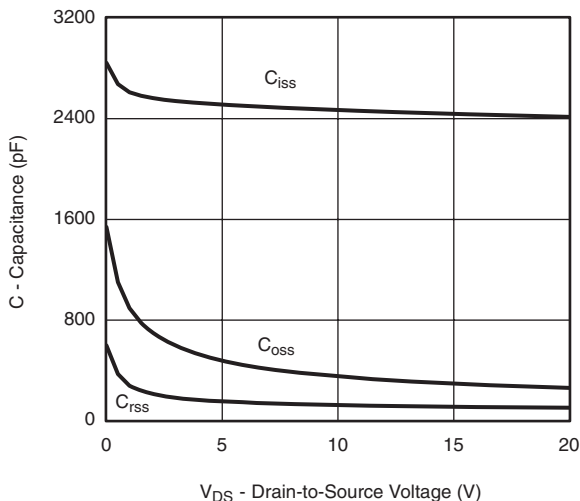
**Transfer Characteristics**



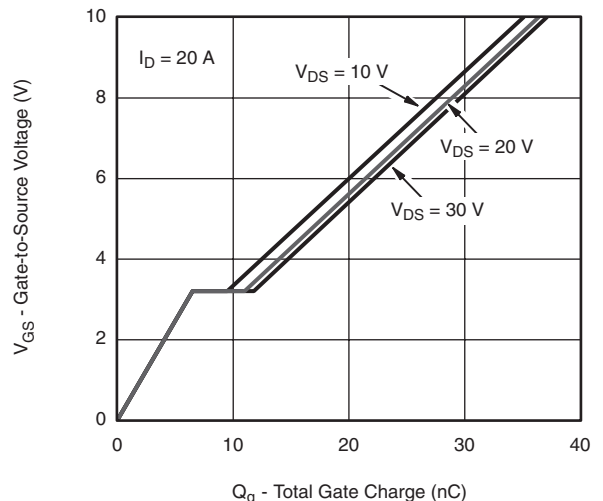
**Transfer Characteristics**



**On-Resistance vs. Drain Current**

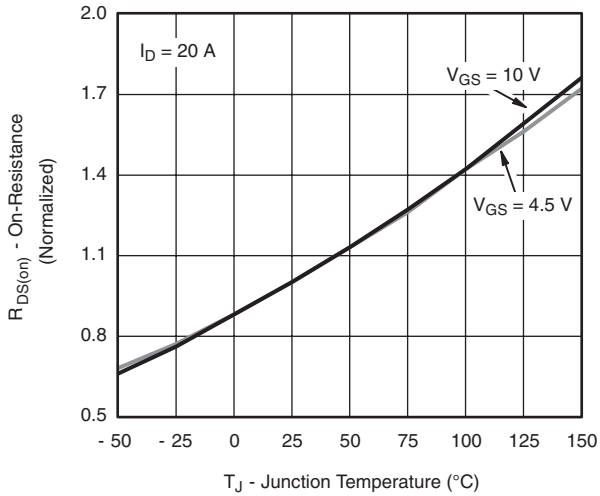


**Capacitance**

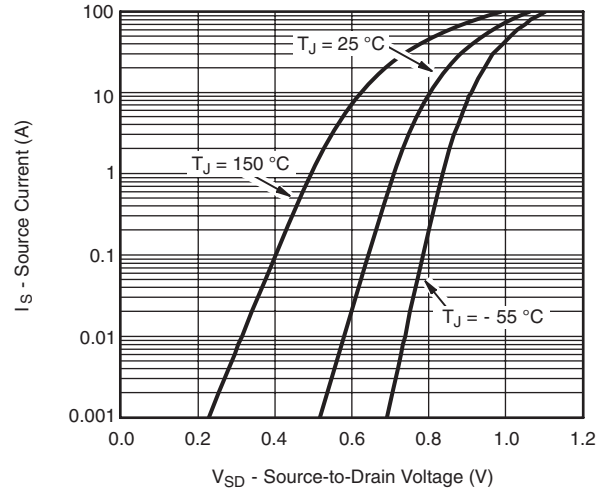


**Gate Charge**

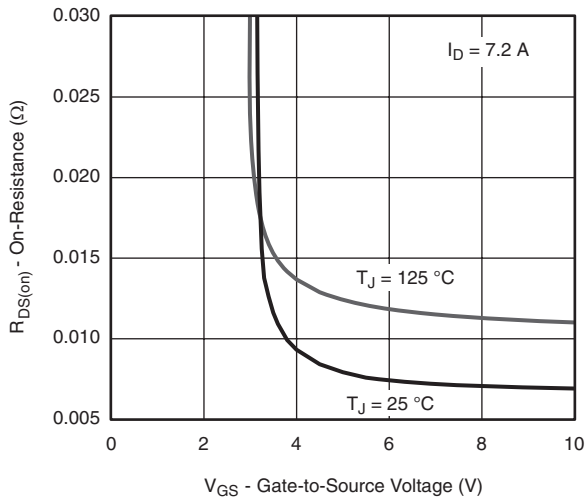
### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



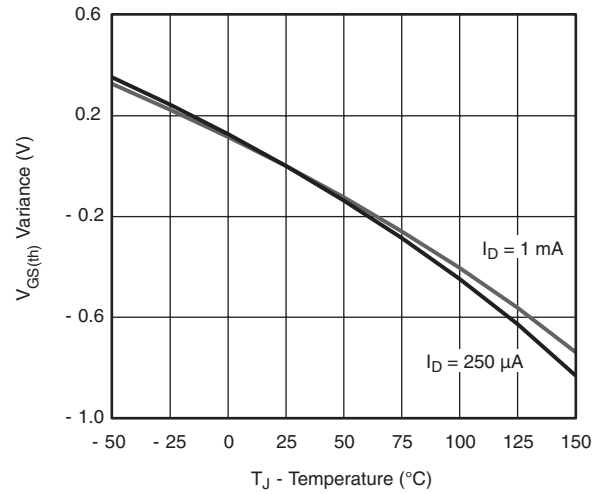
**On-Resistance vs. Junction Temperature**



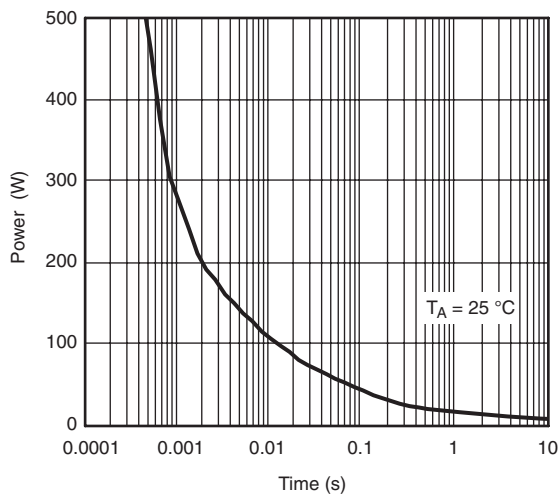
**Source-Drain Diode Forward Voltage**



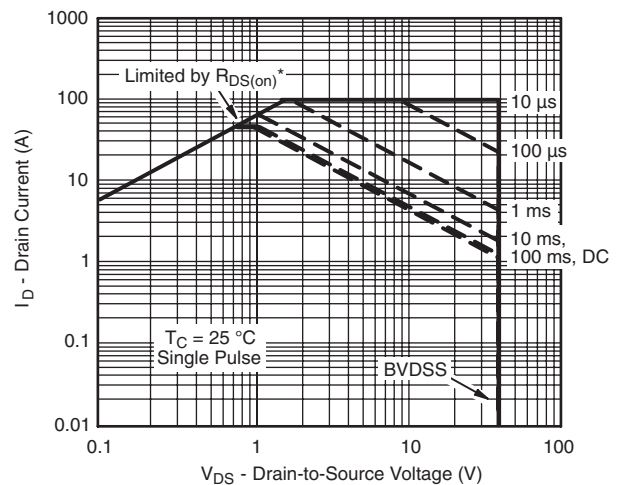
**On-Resistance vs. Gate-to-Source Voltage**



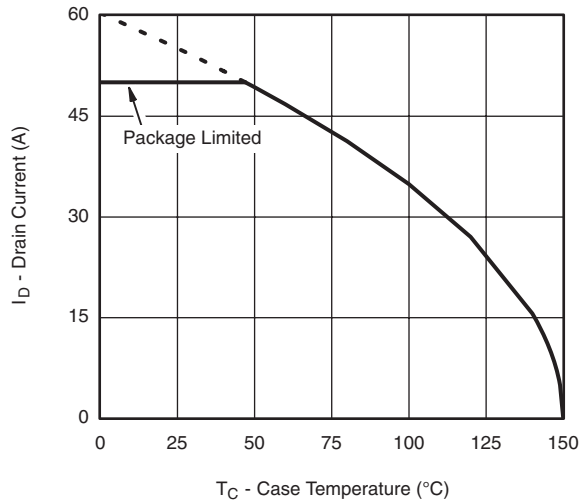
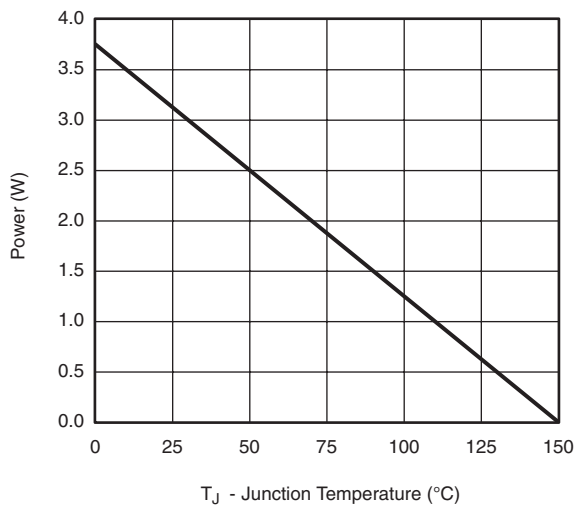
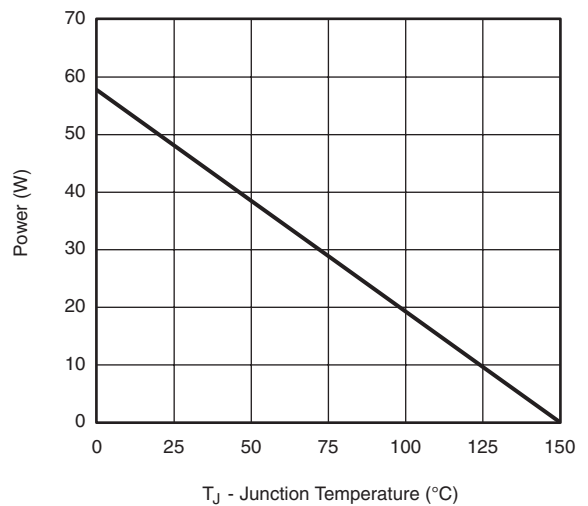
**Threshold Voltage**



**Single Pulse, Junction-to-Ambient**

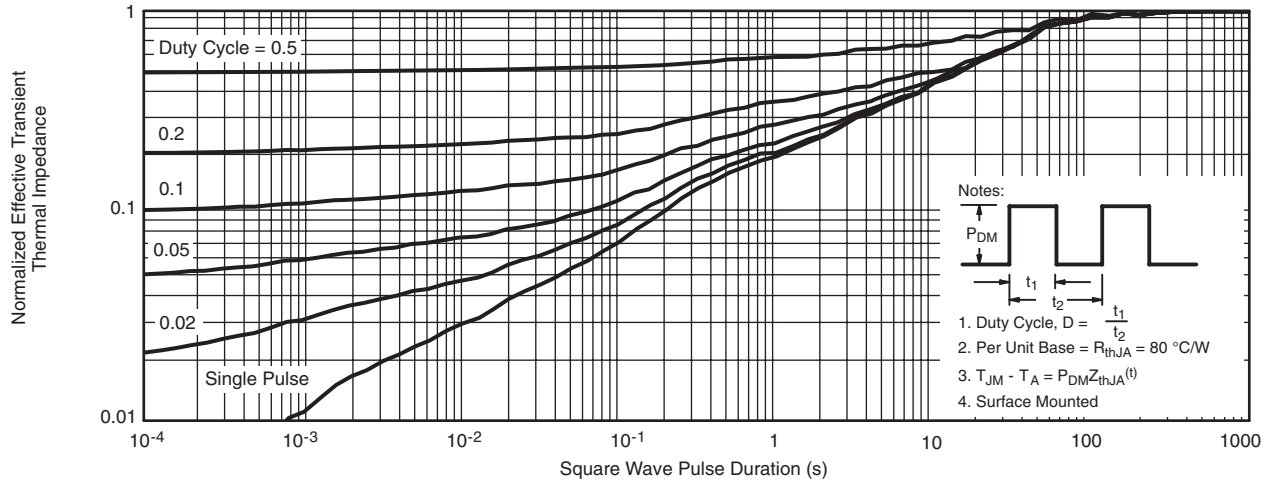


**Safe Operating Area, Junction-to-Case**  
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

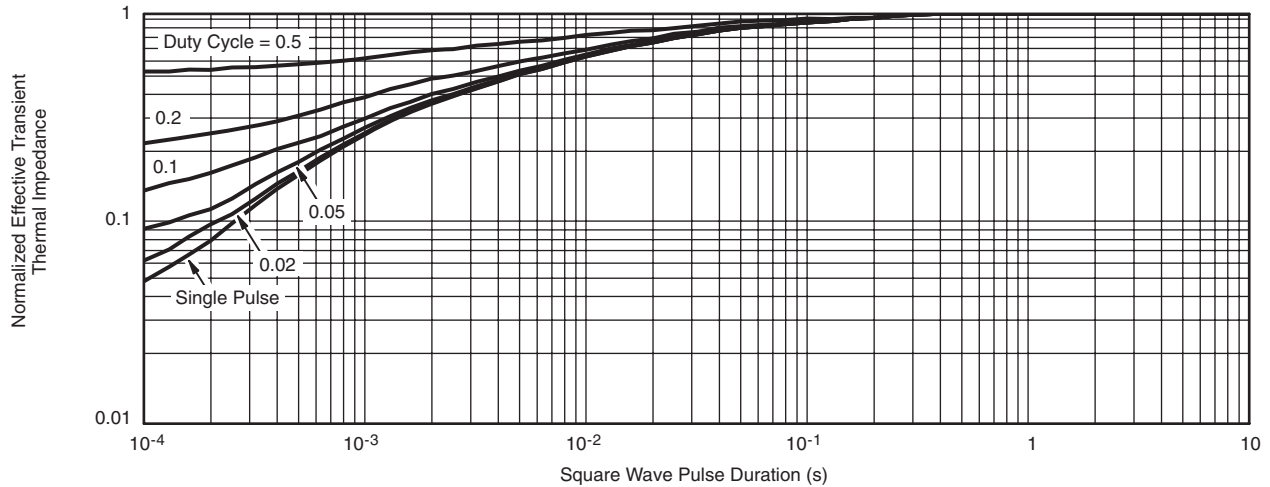
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

**Current Derating\*, Junction-to-Case**

**Power Derating, Junction-to-Ambient**

**Power Derating, Junction-to-Case**

\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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### TO-252AA Case Outline



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T16-0236-Rev. P, 16-May-16 DWG: 5347				

**Notes**

- Dimension L3 is for reference only.

## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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