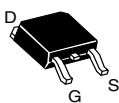
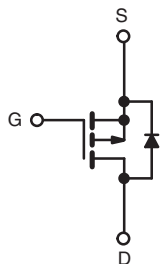
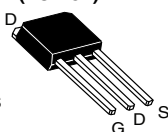


## Power MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V)	- 50
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = - 10$ V   0.28
$Q_g$ (Max.) (nC)	14
$Q_{gs}$ (nC)	6.5
$Q_{gd}$ (nC)	6.5
Configuration	Single

**DPAK (TO-252)**

**IPAK (TO-251)**


P-Channel MOSFET

### FEATURES

- Surface Mountable (Order As IRFR9020, SiHFR9020)
- Straight Lead Option (Order As IRFU9020, SiHFU9020)
- Repetitive Avalanche Ratings
- Dynamic  $dV/dt$  Rating
- Simple Drive Requirements
- Ease of Paralleling
- Material categorization: For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
 COMPLIANT  
 HALOGEN  
**FREE**  
 Available

### DESCRIPTION

The power MOSFET technology is the key to Vishay's advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on-state resistance combined with high transconductance; superior reverse energy and diode recovery  $dV/dt$ .

The power MOSFET transistors also feature all of the well established advantages of MOSFET'S such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters. Surface mount packages enhance circuit performance by reducing stray inductances and capacitance. The TO-252 surface mount package brings the advantages of power MOSFET'S to high volume applications where PC board surface mounting is desirable. The surface mount option IRFR9020, SiHFR9020 is provided on 16mm tape. The straight lead option IRFU9020, SiHFU9020 of the device is called the IPAK (TO-251).

They are well suited for applications where limited heat dissipation is required such as, computers and peripherals, telecommunication equipment, DC/DC converters, and a wide range of consumer products.

ORDERING INFORMATION				
Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free and Halogen-free	SiHFR9020-GE3	SiHFR9020TR-GE3 <sup>a</sup>	SiHFR9020TRL-GE3 <sup>a</sup>	SiHFU9020-GE3
Lead (Pb)-free	IRFR9020PbF	IRFR9020TRPbF <sup>a</sup>	IRFR9020TRLPbF <sup>a</sup>	IRFU9020PbF
	SiHFR9020-E3	SiHFR9020T-E3 <sup>a</sup>	SiHFR9020TL-E3 <sup>a</sup>	SiHFU9020-E3

#### Note

- a. See device orientation.

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	$V_{DS}$	- 50	V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$		
Continuous Drain Current	$V_{GS}$ at - 10 V	$T_C = 25$ °C	- 9.9	A
		$T_C = 100$ °C	- 6.3	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	- 40		
Linear Derating Factor		0.33	W/°C	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	250	mJ	
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$	- 9.9	A	
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	4.2	mJ	
Maximum Power Dissipation	$T_C = 25$ °C	$P_D$	42	W
Peak Diode Recovery $dV/dt$ <sup>c</sup>		$dV/dt$	5.8	V/ns
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature) <sup>d</sup>	for 10 s		300	



#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 16).
- $V_{DD} = - 25$  V, Starting  $T_J = 25$  °C,  $L = 5.1$  mH,  $R_g = 25$   $\Omega$ , Peak  $I_L = - 9.9$  A
- $I_{SD} \leq - 9.9$  A,  $di/dt \leq - 120$  A/ $\mu$ s,  $V_{DD} \leq 40$  V,  $T_J \leq 150$  °C.
- 0.063" (1.6 mm) from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).



THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	$R_{thJA}$	-	-	110	°C/W	
Case-to-Sink	$R_{thCS}$	-	1.7	-		
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	-	3.0		

**SPECIFICATIONS** ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	- 50	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	- 2.0	-	- 4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$	-	-	$\pm 500$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = \text{max. rating}, V_{GS} = 0\text{ V}$	-	-	250	$\mu\text{A}$
		$V_{DS} = 0.8 \times \text{max. rating}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	1000	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = 5.7\text{ A}^b$	-	0.20	0.28	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} \leq -50\text{ V}, I_{DS} = -5.7\text{ A}$	2.3	3.5	-	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = -25\text{ V}, f = 1.0\text{ MHz}, \text{ see fig. 9}$	-	490	-	pF
Output Capacitance	$C_{oss}$		-	320	-	
Reverse Transfer Capacitance	$C_{rss}$		-	70	-	
Total Gate Charge	$Q_g$	$V_{GS} = -10\text{ V}, I_D = -9.7\text{ A}, V_{DS} = 0.8 \times \text{max. rating}, \text{ see fig. 18 (Independent operating temperature)}$	-	9.4	14	nC
Gate-Source Charge	$Q_{gs}$		-	4.3	6.5	
Gate-Drain Charge	$Q_{gd}$		-	4.3	6.5	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -25\text{ V}, I_D = -9.7\text{ A}, R_g = 18\text{ }\Omega, R_D = 2.4\text{ }\Omega, \text{ see fig. 17 (Independent operating temperature)}$	-	8.2	12	ns
Rise Time	$t_r$		-	57	66	
Turn-Off Delay Time	$t_{d(off)}$		-	12	18	
Fall Time	$t_f$		-	25	38	
Internal Drain Inductance	$L_D$		-	4.5	-	
Internal Source Inductance	$L_S$	Between lead, 6 mm (0.25") from package and center of die contact. 	-	7.5	-	nH
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	- 9.9	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	- 40	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = -9.9\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	- 6.3	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = -9.7\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$	56	110	280	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		0.17	0.34	0.85	nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )				

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 16).
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .



## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Fig. 1 - Typical Output Characteristics



Fig. 4 - Maximum Safe Operating Area

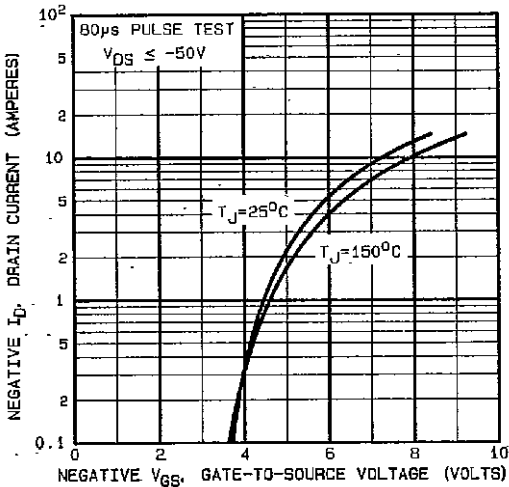


Fig. 2 - Typical Transfer Characteristics



Fig. 5 - Typical Transconductance vs. Drain Current



Fig. 3 - Typical Saturation Characteristics



Fig. 6 - Typical Source-Drain Diode Forward Voltage



Fig. 7 - Breakdown Voltage vs. Temperature



Fig. 9 - Typical Capacitance vs. Drain-to-Source Voltage



Fig. 8 - Normalized On-Resistance vs. Temperature

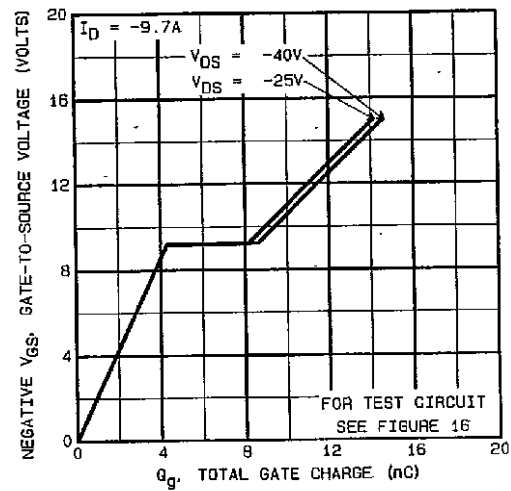


Fig. 10 - Typical Gate Charge vs. Gate-to-Source Voltage



Fig. 11 - Typical On-Resistance vs. Drain Current

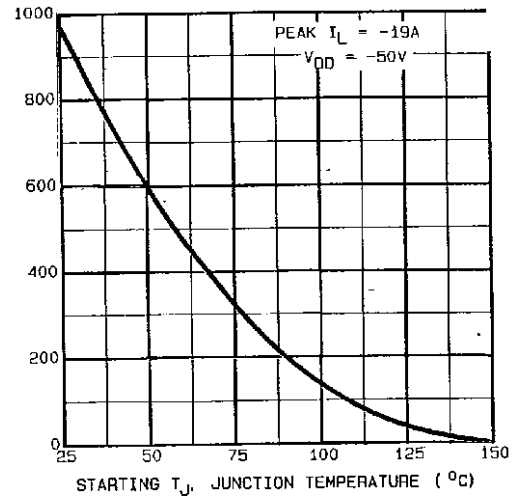


Fig. 13 - Maximum Avalanche vs. Starting Junction Temperature



Fig. 12 - Maximum Drain Current vs. Case Temperature



Fig. 14 - Unclamped Inductive Test Circuit

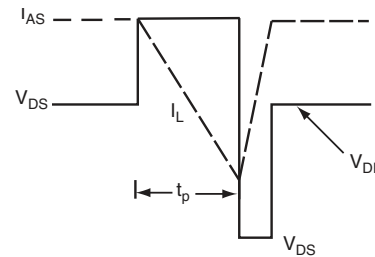


Fig. 15 - Unclamped Inductive Waveforms

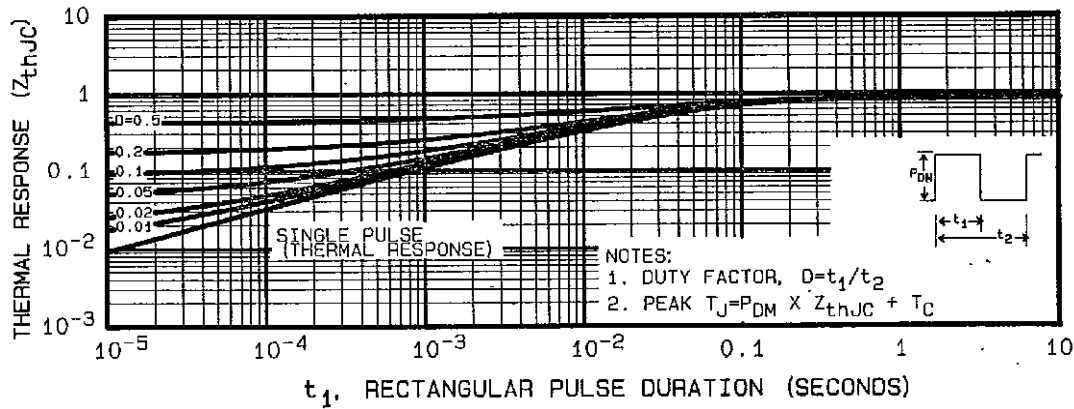


Fig. 16 - Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration



Fig. 17 - Switching Time Waveforms

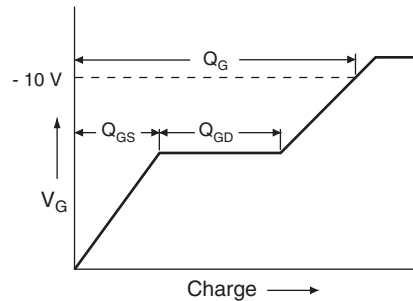


Fig. 19 - Basic Gate Charge Waveform

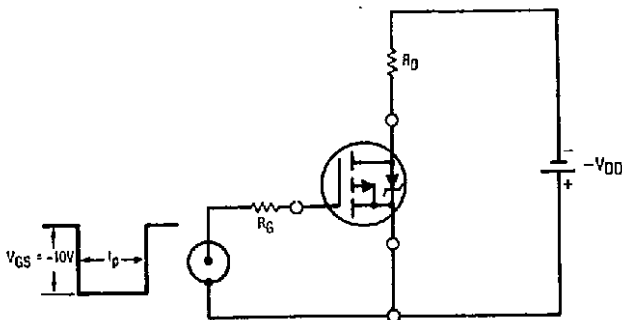


Fig. 18 - Switching Time Test Circuit

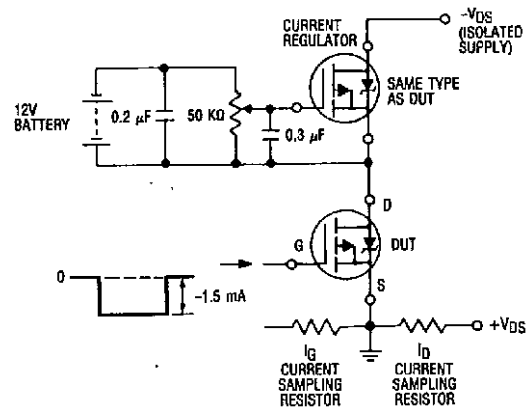
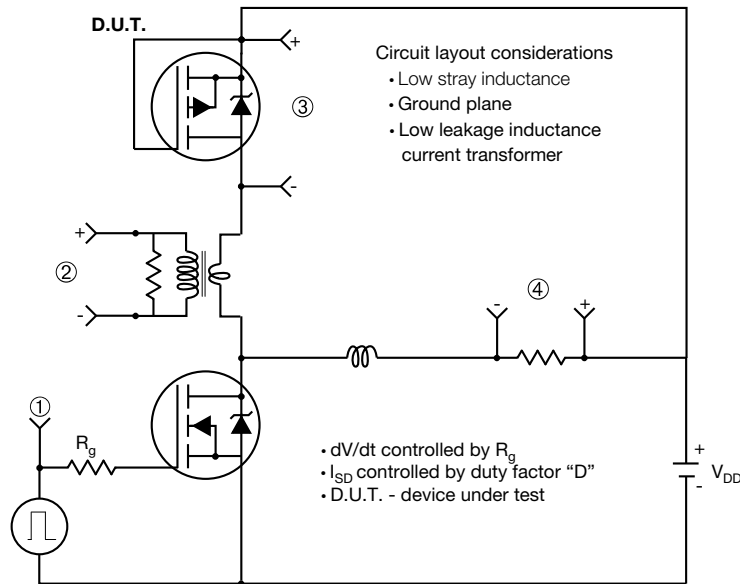


Fig. 20 - Gate Charge Test Circuit

### Peak Diode Recovery dV/dt Test Circuit



**Note**  
 • Compliment N-Channel of D.U.T. for driver



**Note**  
 a.  $V_{GS} = -5\text{ V}$  for logic level and  $-3\text{ V}$  drive devices

**Fig. 21 - For P-Channel**

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### TO-252AA Case Outline



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T16-0236-Rev. P, 16-May-16 DWG: 5347				

**Notes**

- Dimension L3 is for reference only.



### TO-251AA (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.39	0.086	0.094
A1	0.89	1.14	0.035	0.045
b	0.64	0.89	0.025	0.035
b1	0.65	0.79	0.026	0.031
b2	0.76	1.14	0.030	0.045
b3	0.76	1.04	0.030	0.041
b4	4.95	5.46	0.195	0.215
c	0.46	0.61	0.018	0.024
c1	0.41	0.56	0.016	0.022
c2	0.46	0.86	0.018	0.034
D	5.97	6.22	0.235	0.245

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
e	2.29 BSC		2.29 BSC	
L	8.89	9.65	0.350	0.380
L1	1.91	2.29	0.075	0.090
L2	0.89	1.27	0.035	0.050
L3	1.14	1.52	0.045	0.060
theta1	0'	15'	0'	15'
theta2	25'	35'	25'	35'

ECN: S-82111-Rev. A, 15-Sep-08  
DWG: 5968

#### Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension are shown in inches and millimeters.
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.13 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
4. Thermal pad contour optional with dimensions b4, L2, E1 and D1.
5. Lead dimension uncontrolled in L3.
6. Dimension b1, b3 and c1 apply to base metal only.
7. Outline conforms to JEDEC outline TO-251AA.

## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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