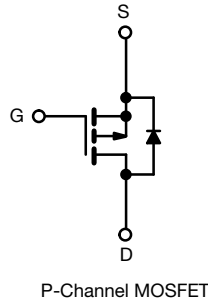
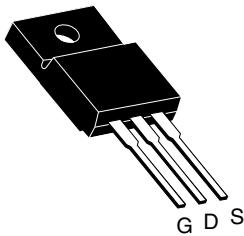


Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	-100	
$R_{DS(on)}$ (Ω)	$V_{GS} = -10$ V	0.30
Q_g max. (nC)	38	
Q_{gs} (nC)	6.8	
Q_{gd} (nC)	21	
Configuration	Single	

TO-220 FULLPAK


FEATURES

- Isolated package
- High voltage isolation = 2.5 kV_{RMS} (t = 60 s; f = 60 Hz)
- Sink to lead creepage distance = 4.8 mm
- P-channel
- 175 °C operating temperature
- Dynamic dV/dt rating
- Low thermal resistance
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS*
Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 FULLPAK eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The FULLPAK is mounted to a heatsink using a single clip or by a single screw fixing.

ORDERING INFORMATION	
Package	TO-220 FULLPAK
Lead (Pb)-free	IRFI9530GPbF
	SiHFI9530G-E3
SnPb	IRFI9530G
	SiHFI9530G



ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	-100	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	V_{GS} at -10 V	$T_C = 25$ °C	-7.7
		$T_C = 100$ °C	-5.4
Pulsed Drain Current ^a	I_{DM}	-31	A
Linear Derating Factor		0.28	W/°C
Single Pulse Avalanche Energy ^b	E_{AS}	380	mJ
Repetitive Avalanche Current ^a	I_{AR}	-7.7	A
Repetitive Avalanche Energy ^a	E_{AR}	4.2	mJ
Maximum Power Dissipation	$T_C = 25$ °C	P_D	42
Peak Diode Recovery dV/dt ^c		dV/dt	-5.5
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +175	°C
Soldering Recommendations (Peak temperature) ^d	for 10 s	300	
Mounting Torque	6-32 or M3 screw		10
			1.1
			lbf · in
			N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = -25$ V, starting $T_J = 25$ °C, L = 9.6 mH, $R_G = 25$ Ω , $I_{AS} = -7.7$ A (see fig. 12).
- $I_{SD} \leq -7.7$ A, $dI/dt \leq 140$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 175$ °C.
- 1.6 mm from case.



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	65	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	3.6	

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		-100	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}, I_D = 1\text{ mA}$		-	-0.10	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		-2.0	-	-4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -100\text{ V}, V_{GS} = 0\text{ V}$		-	-	-100	μA
		$V_{DS} = -80\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$		-	-	-500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$	$I_D = -4.6\text{ A}^b$	-	-	0.30	Ω
Forward Transconductance	g_{fs}	$V_{DS} = -50\text{ V}, I_D = -4.6\text{ A}^b$		3.4	-	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = -25\text{ V}, f = 1.0\text{ MHz}, \text{ see fig. 5}$		-	860	-	μF
Output Capacitance	C_{oss}			-	340	-	
Reverse Transfer Capacitance	C_{rss}			-	93	-	
Drain to Sink Capacitance	C	$f = 1.0\text{ MHz}$		-	12	-	
Total Gate Charge	Q_g	$V_{GS} = -10\text{ V}$	$I_D = -12\text{ A}, V_{DS} = -80\text{ V}, \text{ see fig. 6 and 13}^b$	-	-	38	nC
Gate-Source Charge	Q_{gs}			-	-	6.8	
Gate-Drain Charge	Q_{gd}			-	-	21	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -50\text{ V}, I_D = -12\text{ A}, R_G = 12\text{ }\Omega, R_D = 3.9\text{ }\Omega, \text{ see fig. 10}^b$		-	12	-	ns
Rise Time	t_r			-	52	-	
Turn-Off Delay Time	$t_{d(off)}$			-	31	-	
Fall Time	t_f			-	39	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	L_S			-	7.5	-	
Gate Input Resistance	R_g	$f = 1\text{ MHz}, \text{ open drain}$		0.4	-	3.3	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p-n junction diode 		-	-	-7.7	A
Pulsed Diode Forward Current ^a	I_{SM}			-	-	-31	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = -7.7\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	-6.3	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = -12\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$		-	120	240	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	0.46	0.92	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

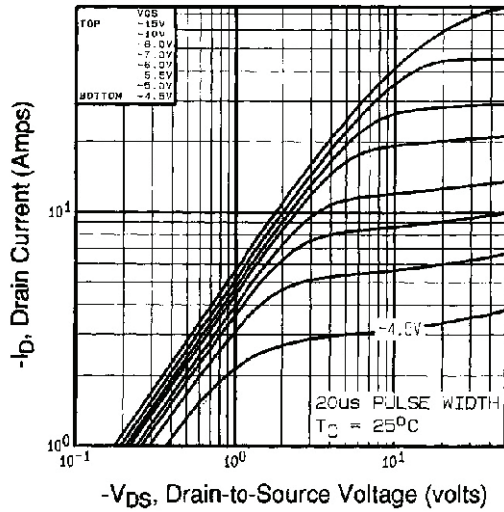


Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ\text{C}$

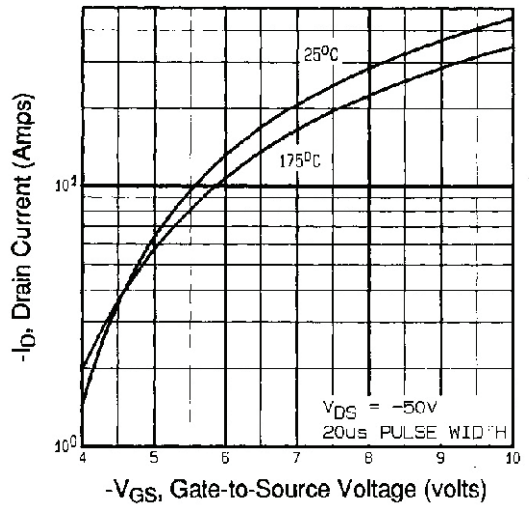


Fig. 3 - Typical Transfer Characteristics

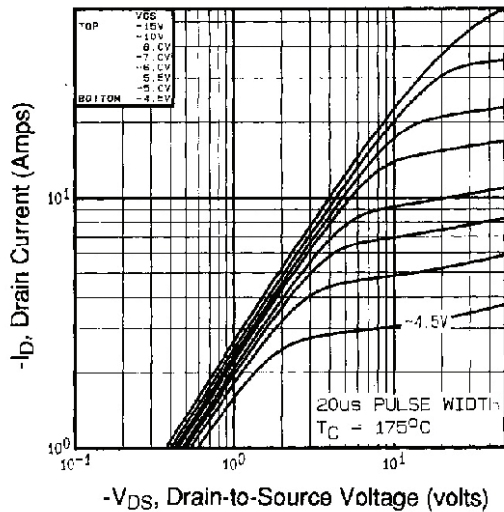


Fig. 2 - Typical Output Characteristics, $T_C = 175^\circ\text{C}$

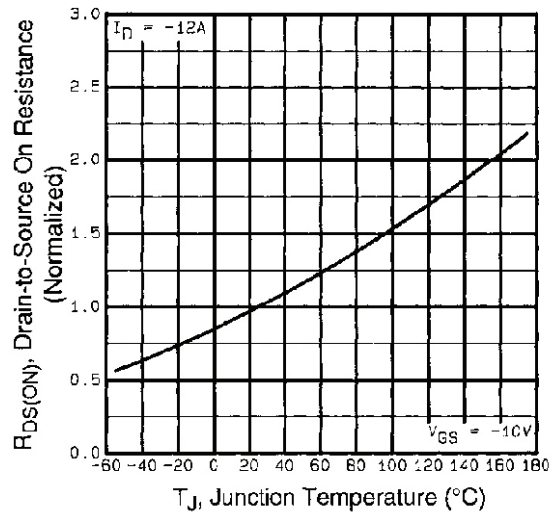


Fig. 4 - Normalized On-Resistance vs. Temperature

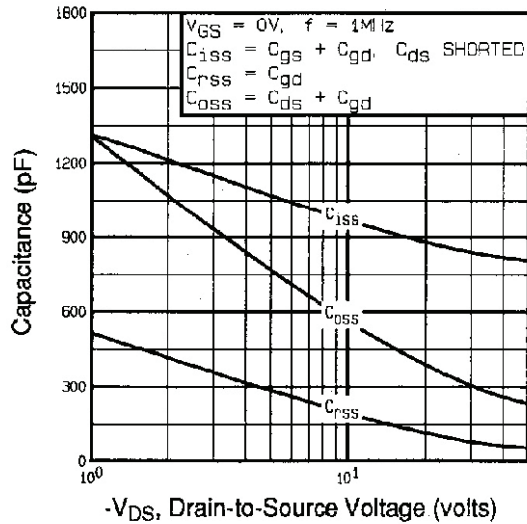


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

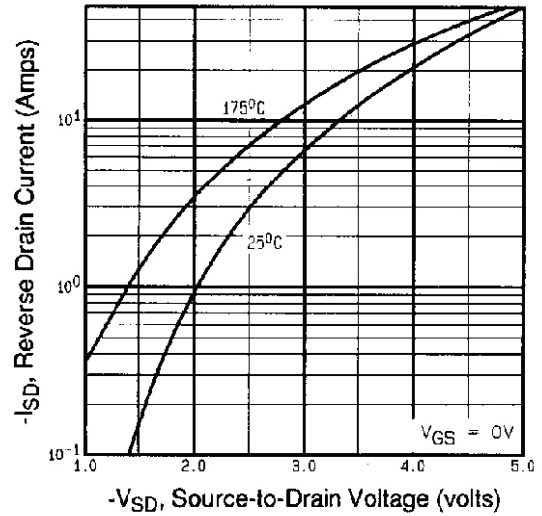


Fig. 7 - Typical Source-Drain Diode Forward Voltage

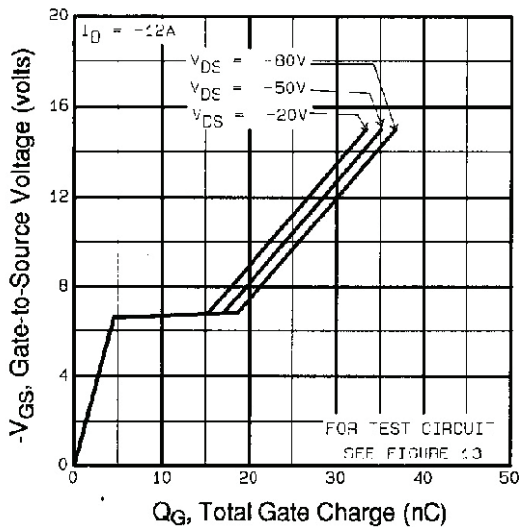


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

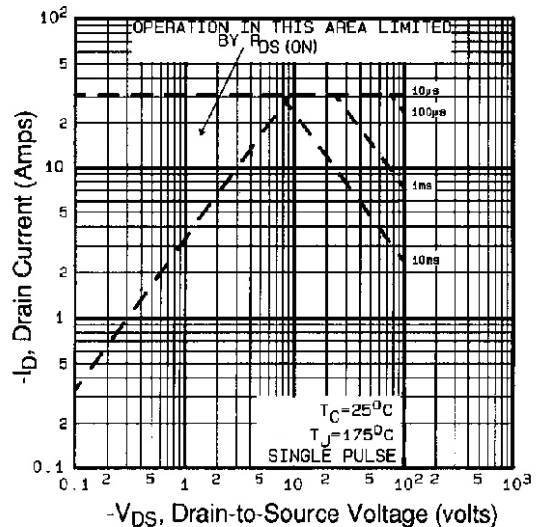


Fig. 8 - Maximum Safe Operating Area

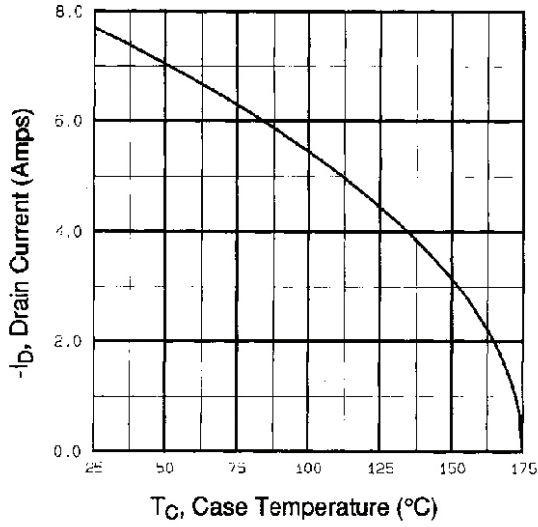


Fig. 9 - Maximum Drain Current vs. Case Temperature

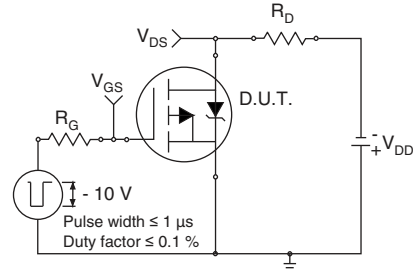


Fig. 10a - Switching Time Test Circuit

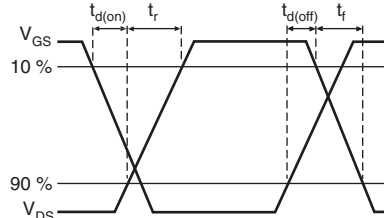


Fig. 10b - Switching Time Waveforms

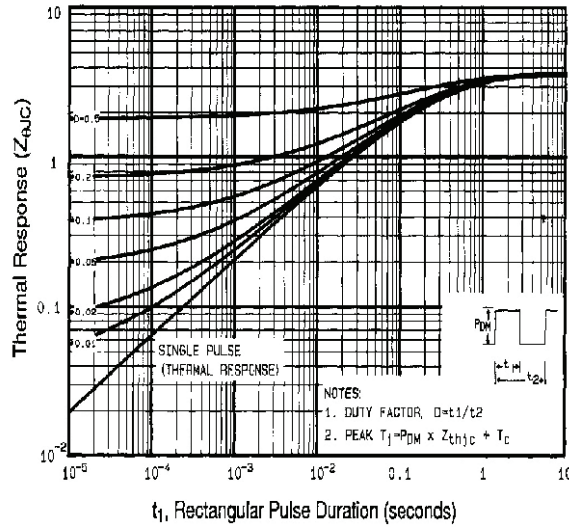


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

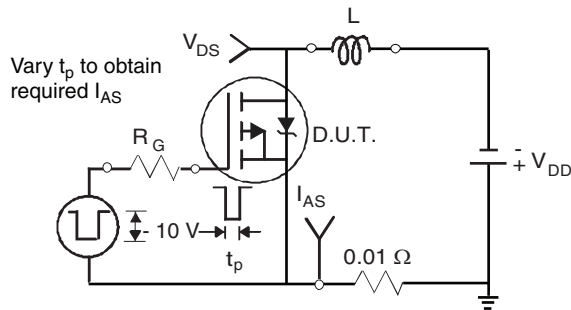


Fig. 12a - Unclamped Inductive Test Circuit

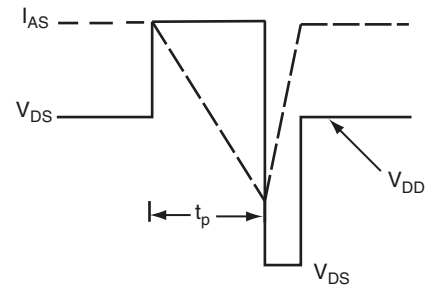


Fig. 12b - Unclamped Inductive Waveforms

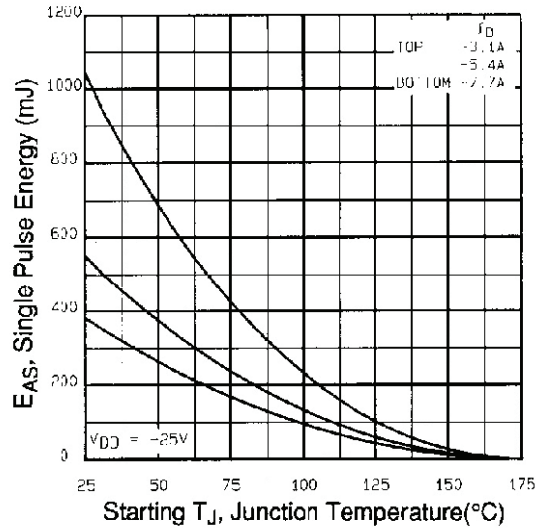


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

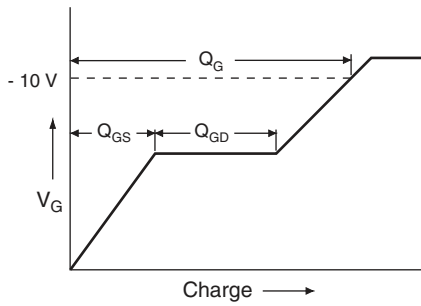


Fig. 13a - Basic Gate Charge Waveform

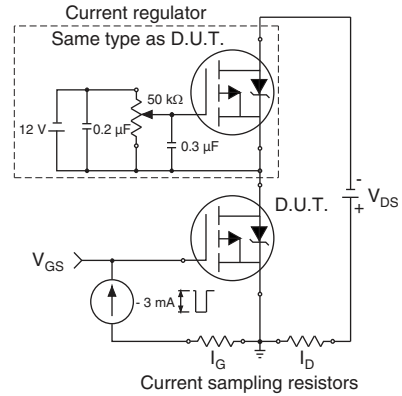


Fig. 13b - Gate Charge Test Circuit

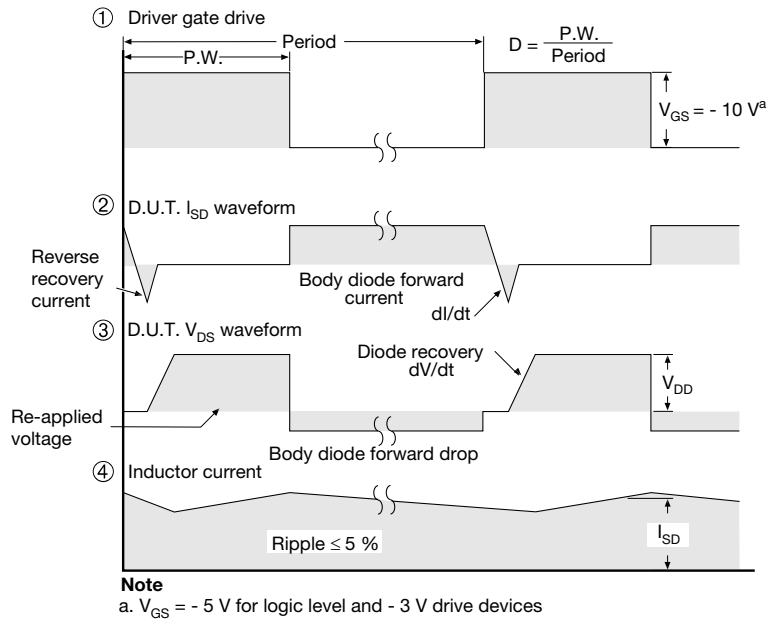
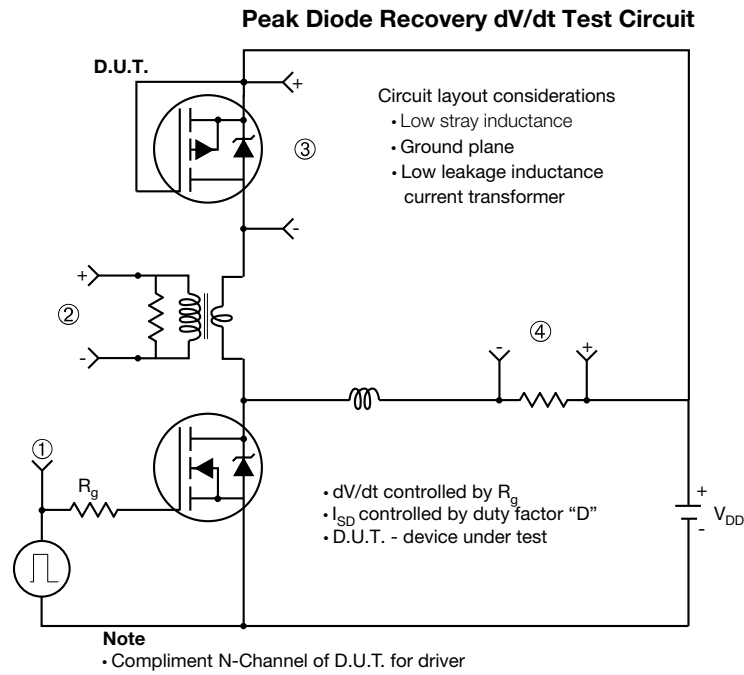


Fig.14 - For P-Channel

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