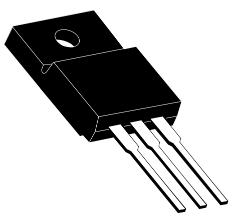
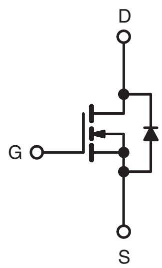
# E Series Power MOSFET

| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{DS}$ (V) at $T_J$ max. | 700 | |
| $R_{DS(on)}$ max. at 25 °C (Ω) | $V_{GS}$ = 10 V | 0.6 |
| $Q_g$ max. (nC) | 48 | |
| $Q_{gs}$ (nC) | 6 | |
| $Q_{gd}$ (nC) | 11 | |
| Configuration | Single | |

TO-220 FULLPAK



G D S




N-Channel MOSFET

## FEATURES

- Low figure-of-merit (FOM) $R_{on}$ x $Q_g$
- Low input capacitance ($C_{iss}$)
- Reduced switching and conduction losses
- Ultra low gate charge ($Q_g$)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

## APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Renewable energy
  - Solar (PV inverters)

| ORDERING INFORMATION | |
|---|---|
| Package | TO-220 FULLPAK |
| Lead (Pb)-free and Halogen-free | SiHF6N65E-GE3 |

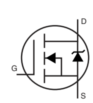
**ABSOLUTE MAXIMUM RATINGS** ($T_C$ = 25 °C, unless otherwise noted)

| PARAMETER | | | SYMBOL | LIMIT | UNIT |
|---|---|---|---|---|---|
| Drain-Source Voltage | | | $V_{DS}$ | 650 | V |
| Gate-Source Voltage | | | $V_{GS}$ | ± 30 | |
| Continuous Drain Current ($T_J$ = 150 °C) [e] | $V_{GS}$ at 10 V | $T_C$ = 25 °C | $I_D$ | 7 | A |
| | | $T_C$ = 100 °C | | 5 | |
| Pulsed Drain Current [a] | | | $I_{DM}$ | 18 | |
| Linear Derating Factor | | | | 0.63 | W/°C |
| Single Pulse Avalanche Energy [b] | | | $E_{AS}$ | 56 | mJ |
| Maximum Power Dissipation | | | $P_D$ | 31 | W |
| Operating Junction and Storage Temperature Range | | | $T_J$, $T_{stg}$ | -55 to +150 | °C |
| Drain-Source Voltage Slope | $T_J$ = 125 °C | | dV/dt | 37 | V/ns |
| Reverse Diode dV/dt [d] | | | | 27 | |
| Soldering Recommendations (Peak Temperature) [c] | for 10 s | | | 300 | °C |

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature.
b. $V_{DD}$ = 50 V, starting $T_J$ = 25 °C, L = 28.2 mH, $R_g$ = 25 Ω, $I_{AS}$ = 2 A.
c. 1.6 mm from case.
d. $I_{SD} \leq I_D$, dI/dt = 100 A/μs, starting $T_J$ = 25 °C.
e. Limited by maximum junction temperature.

| THERMAL RESISTANCE RATINGS | | | | |
|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TYP.** | **MAX.** | **UNIT** |
| Maximum Junction-to-Ambient | $R_{thJA}$ | - | 65 | °C/W |
| Maximum Junction-to-Case (Drain) | $R_{thJC}$ | - | 4.0 | |

| **SPECIFICATIONS** ($T_J$ = 25 °C, unless otherwise noted) | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 μA | 650 | - | - | V |
| $V_{DS}$ Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to 25 °C, $I_D$ = 1 mA | - | 0.73 | - | V/°C |
| Gate-Source Threshold Voltage (N) | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | 2 | - | 4 | V |
| Gate-Source Leakage | $I_{GSS}$ | $V_{GS}$ = ± 20 V | - | - | ± 100 | nA |
| | | $V_{GS}$ = ± 30 V | - | - | ± 1 | μA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 650 V, $V_{GS}$ = 0 V | - | - | 1 | μA |
| | | $V_{DS}$ = 520 V, $V_{GS}$ = 0 V, $T_J$ = 125 °C | - | - | 10 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V; $I_D$ = 3 A | - | 0.5 | 0.6 | Ω |
| Forward Transconductance | $g_{fs}$ | $V_{DS}$ = 30 V, $I_D$ = 3 A | - | 2 | - | S |
| **Dynamic** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 100 V, f = 1 MHz | - | 820 | - | pF |
| Output Capacitance | $C_{oss}$ | | - | 40 | - | |
| Reverse Transfer Capacitance | $C_{rss}$ | | - | 4 | - | |
| Effective Output Capacitance, Energy Related [a] | $C_{o(er)}$ | $V_{DS}$ = 0 V to 520 V, $V_{GS}$ = 0 V | - | 36 | - | |
| Effective Output Capacitance, Time Related [b] | $C_{o(tr)}$ | | - | 117 | - | |
| Total Gate Charge | $Q_g$ | $V_{GS}$ = 10 V; $I_D$ = 3 A, $V_{DS}$ = 520 V | - | 24 | 48 | nC |
| Gate-Source Charge | $Q_{gs}$ | | - | 6 | - | |
| Gate-Drain Charge | $Q_{gd}$ | | - | 11 | - | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 520 V, $I_D$ = 3 A, $V_{GS}$ = 10 V, $R_g$ = 9.1 Ω | - | 14 | 28 | ns |
| Rise Time | $t_r$ | | - | 12 | 24 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 30 | 60 | |
| Fall Time | $t_f$ | | - | 20 | 40 | |
| Gate Input Resistance | $R_g$ | f = 1 MHz, open drain | - | 1.4 | - | Ω |
| **Drain-Source Body Diode Characteristics** | | | | | | |
| Continuous Source-Drain Diode Current | $I_S$ | MOSFET symbol showing the integral reverse p - n junction diode  | - | - | 7 | A |
| Pulsed Diode Forward Current | $I_{SM}$ | | - | - | 18 | |
| Diode Forward Voltage | $V_{SD}$ | $T_J$ = 25 °C, $I_S$ = 3 A, $V_{GS}$ = 0 V | - | - | 1.3 | V |
| Reverse Recovery Time | $t_{rr}$ | $T_J$ = 25 °C, $I_F$ = $I_S$ = 3 A, dI/dt = 100 A/μs, $V_R$ = 25 V | - | 237 | - | ns |
| Reverse Recovery Charge | $Q_{rr}$ | | - | 2.2 | - | μC |
| Reverse Recovery Current | $I_{RRM}$ | | - | 16 | - | A |

**Notes**

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as $C_{oss}$ while $V_{DS}$ is rising from 0 % to 80 % $V_{DSS}$.

b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 % to 80 % $V_{DSS}$.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

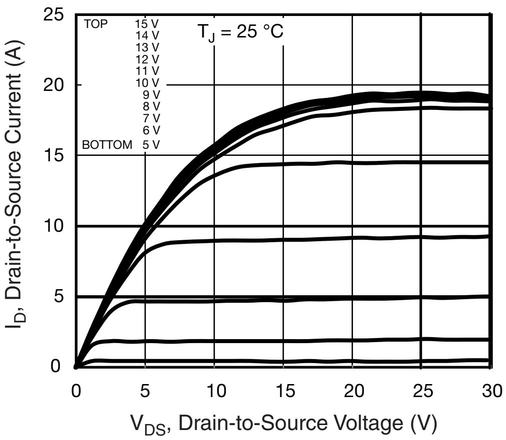



**Fig. 1 - Typical Output Characteristics**

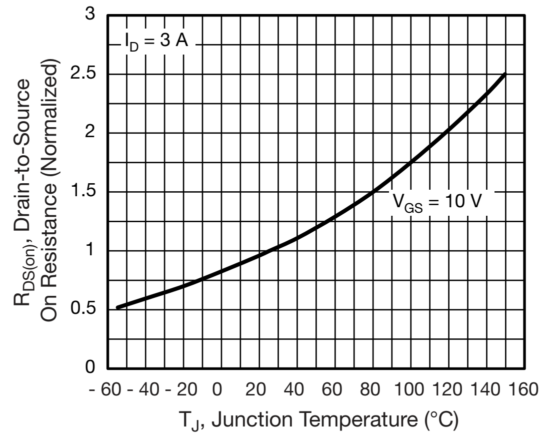



**Fig. 4 - Normalized On-Resistance vs. Temperature**

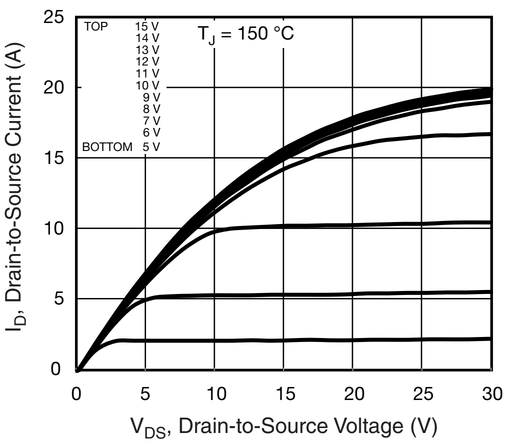



**Fig. 2 - Typical Output Characteristics**

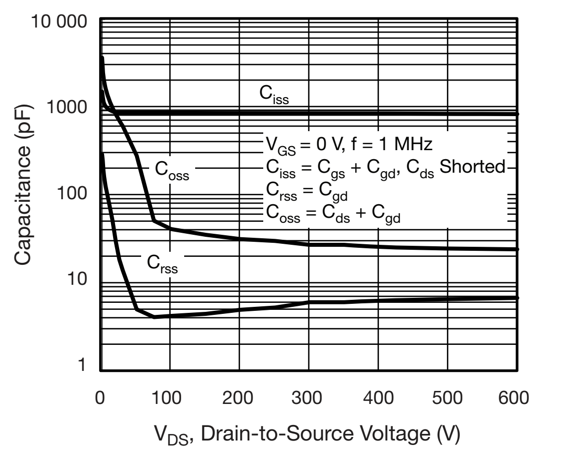



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

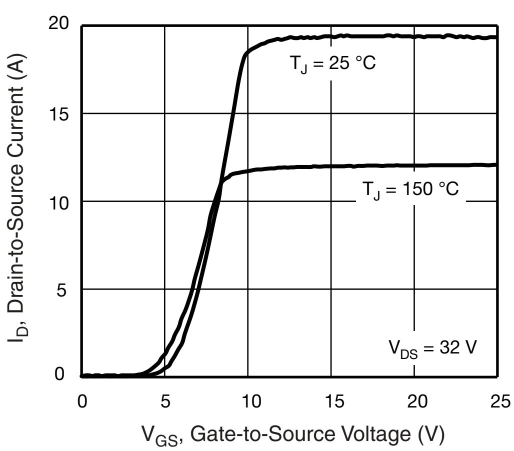



**Fig. 3 - Typical Transfer Characteristics**

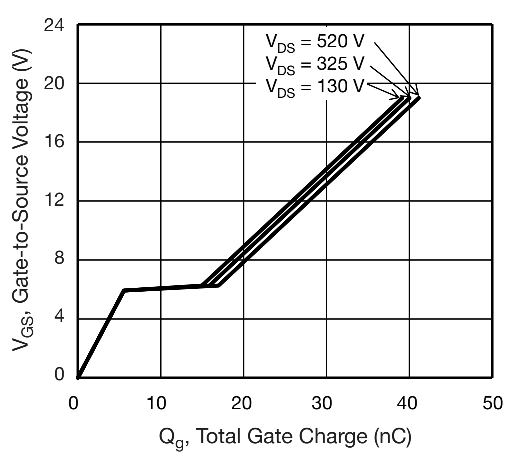



**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**

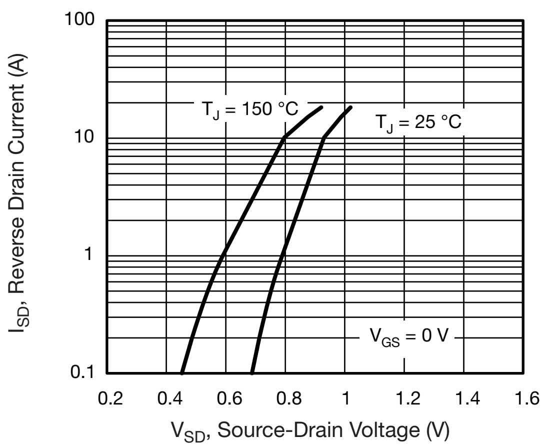



**Fig. 7 - Typical Source-Drain Diode Forward Voltage**

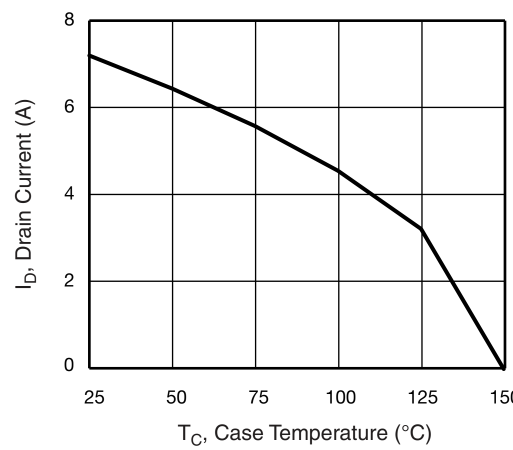
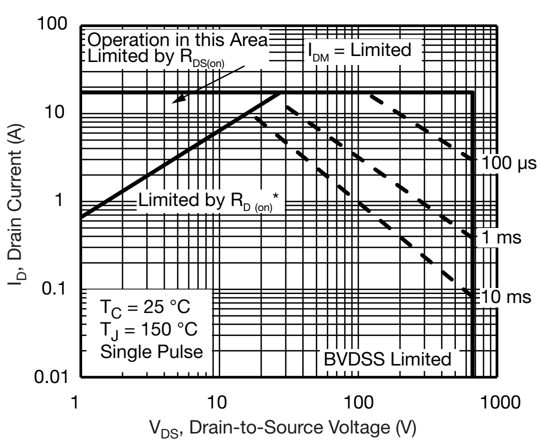



**Fig. 9 - Maximum Drain Current vs. Case Temperature**




* $V_{GS}$ > minimum $V_{GS}$ at which $R_{DS(on)}$ is specified

**Fig. 8 - Maximum Safe Operating Area**

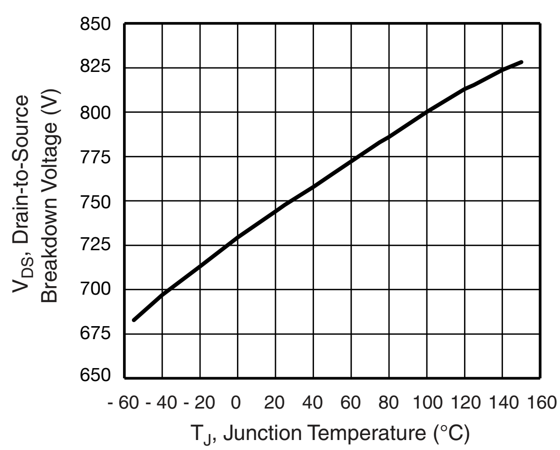



**Fig. 10 - Temperature vs. Drain-to-Source Voltage**

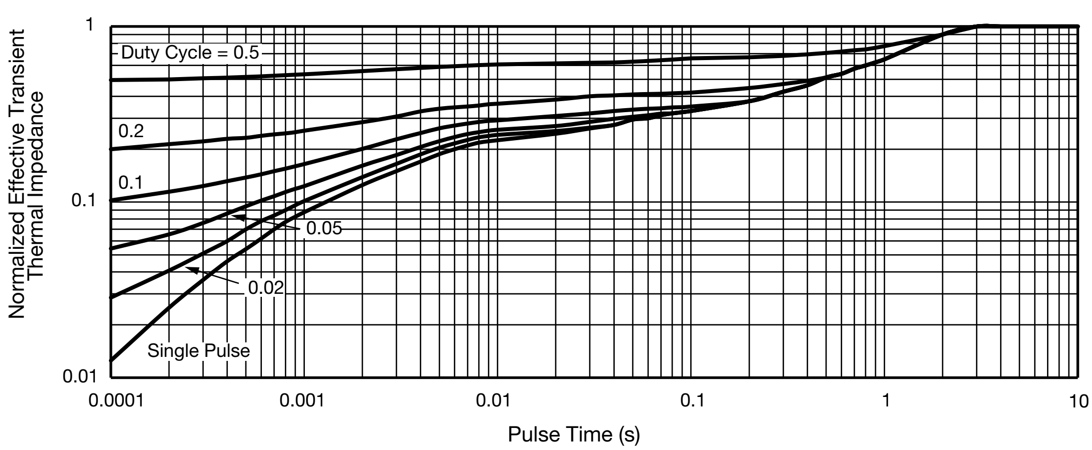



**Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case**

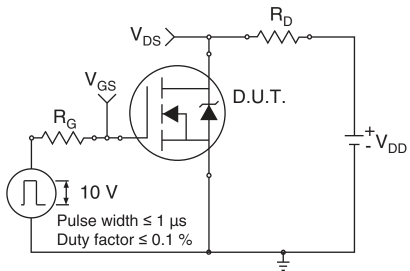



**Fig. 12 - Switching Time Test Circuit**

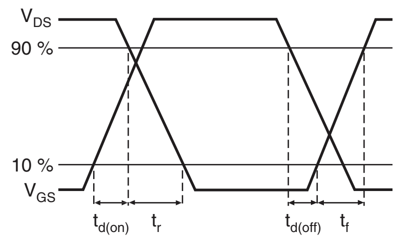



**Fig. 13 - Switching Time Waveforms**

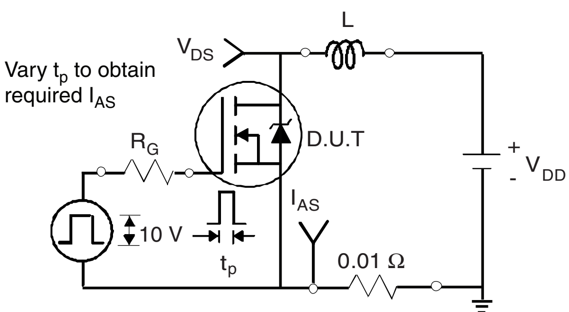



**Fig. 14 - Unclamped Inductive Test Circuit**

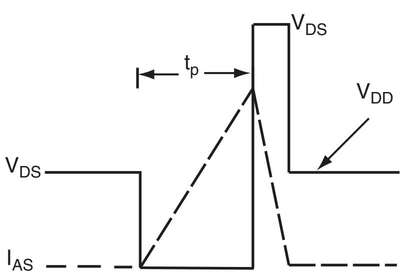



**Fig. 15 - Unclamped Inductive Waveforms**

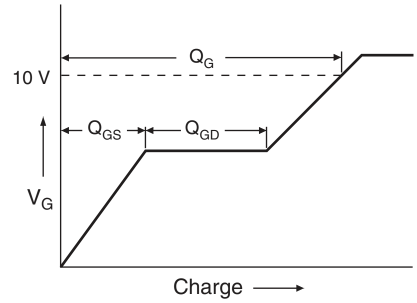



**Fig. 16 - Basic Gate Charge Waveform**

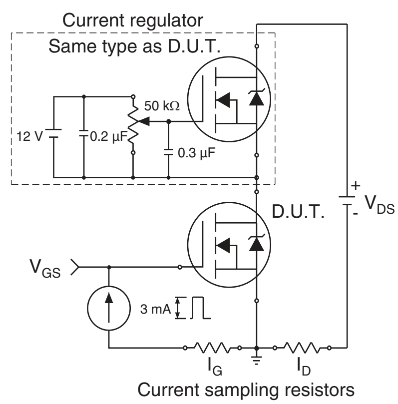
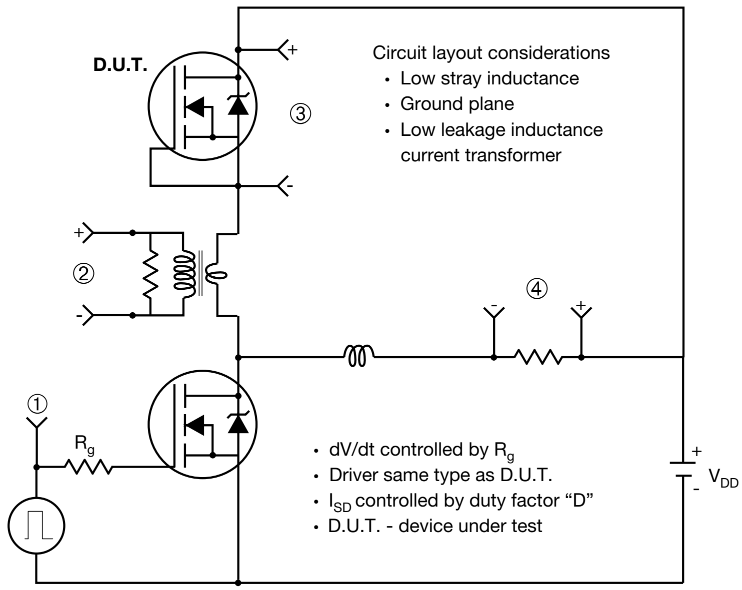
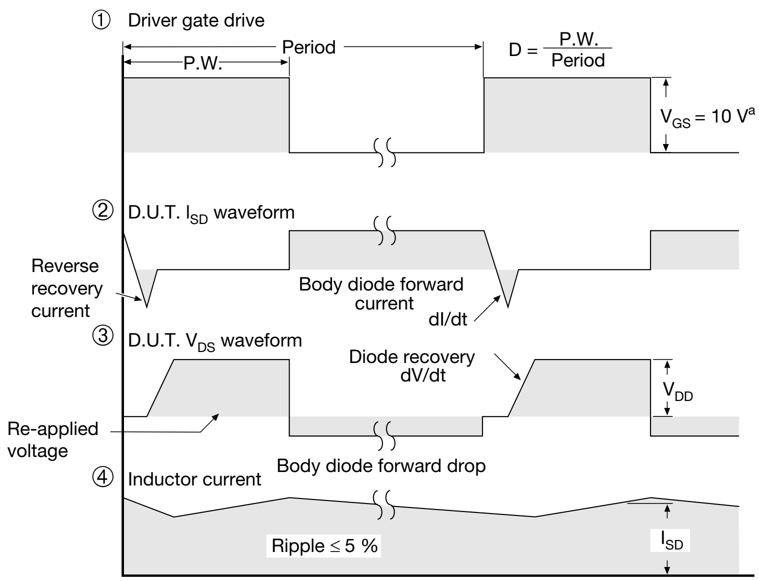



**Fig. 17 - Gate Charge Test Circuit**


For technical questions, contact: hvm@vishay.com

**Peak Diode Recovery dV/dt Test Circuit**



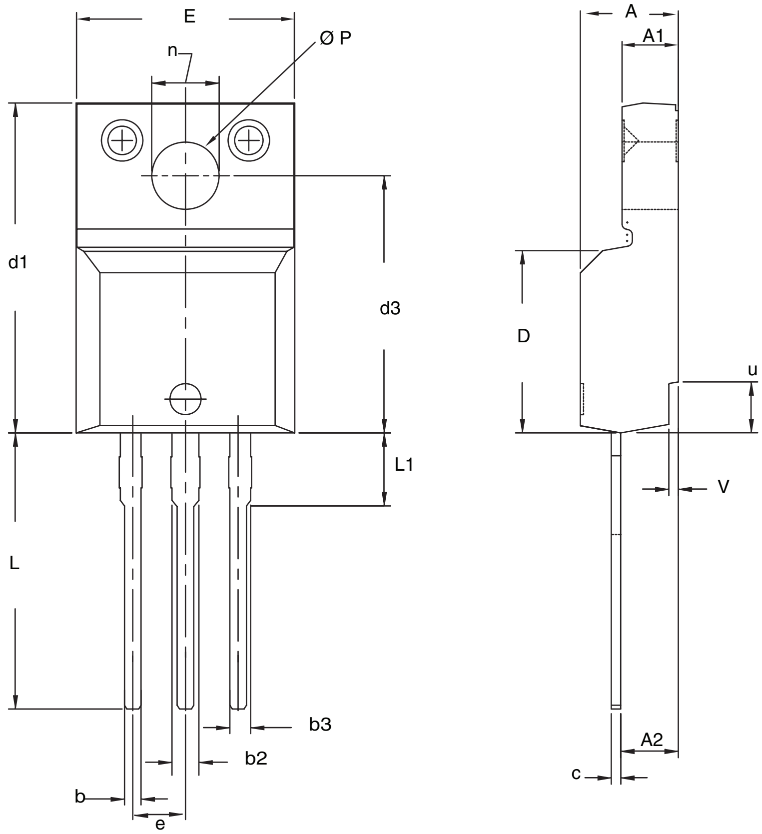

**Note**

a. $V_{GS}$ = 5 V for logic level devices

**Fig. 18 - For N-Channel**

*Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91547.*

### TO-220 FULLPAK (HIGH VOLTAGE)




| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM. | MIN. | MAX. | MIN. | MAX. |
| A | 4.570 | 4.830 | 0.180 | 0.190 |
| A1 | 2.570 | 2.830 | 0.101 | 0.111 |
| A2 | 2.510 | 2.850 | 0.099 | 0.112 |
| b | 0.622 | 0.890 | 0.024 | 0.035 |
| b2 | 1.229 | 1.400 | 0.048 | 0.055 |
| b3 | 1.229 | 1.400 | 0.048 | 0.055 |
| c | 0.440 | 0.629 | 0.017 | 0.025 |
| D | 8.650 | 9.800 | 0.341 | 0.386 |
| d1 | 15.88 | 16.120 | 0.622 | 0.635 |
| d3 | 12.300 | 12.920 | 0.484 | 0.509 |
| E | 10.360 | 10.630 | 0.408 | 0.419 |
| e | 2.54 BSC | | 0.100 BSC | |
| L | 13.200 | 13.730 | 0.520 | 0.541 |
| L1 | 3.100 | 3.500 | 0.122 | 0.138 |
| n | 6.050 | 6.150 | 0.238 | 0.242 |
| Ø P | 3.050 | 3.450 | 0.120 | 0.136 |
| u | 2.400 | 2.500 | 0.094 | 0.098 |
| v | 0.400 | 0.500 | 0.016 | 0.020 |
| ECN: X09-0126-Rev. B, 26-Oct-09<br>DWG: 5972 | | | | |

**Notes**
1. To be used only for process drawing.
2. These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads.
3. All critical dimensions should C meet $C_{pk} > 1.33$.
4. All dimensions include burrs and plating thickness.
5. No chipping or package damage.

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