



# Quad Complementary CMOS Analog Switch

## FEATURES

- $\pm 22\text{-V}$  Supply Voltage Rating
- TTL and CMOS Compatible Logic
- Low On-Resistance— $r_{DS(on)}$ :  $45\ \Omega$
- Low Leakage— $I_{D(on)}$ :  $20\ \text{pA}$
- Single Supply Operation Possible
- Extended Temperature Range
- Fast Switching— $t_{ON}$ :  $85\ \text{ns}$

## BENEFITS

- Low Charge Injection— $Q$ :  $1\ \text{pC}$
- Wide Analog Signal Range
- Simple Logic Interface
- Higher Accuracy
- Minimum Transients
- Reduced Power Consumption
- Low Cost

## APPLICATIONS

- Industrial Instrumentation
- Test Equipment
- Communications Systems
- Computer Peripherals
- Portable Instruments
- Sample-and-Hold Circuits

## DESCRIPTION

The versatile DG213 analog switch has two NC and two NO switches. It can be used in various configurations, including four single-pole single-throw (SPST), two single-pole double-throw (SPDT), one "T" switch, one DPDT, etc. This device is fabricated in a Vishay Siliconix' proprietary high-voltage silicon gate CMOS process, resulting in lower on-resistance, lower leakage, higher speed, and lower power consumption.

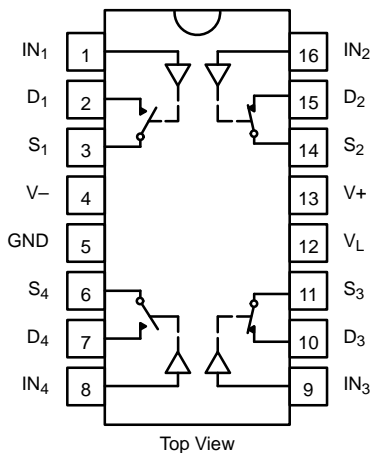
injection compensation design minimizes switching transients. These switches can handle up to  $\pm 22\ \text{V}$ , and have an improved continuous current rating of  $30\ \text{mA}$ . An epitaxial layer prevents latchup.

All switches feature true bi-directional performance in the on condition, and will block signals to the supply levels in the off condition.

This analog switch was designed for a wide variety of general purpose applications in telecommunications, instrumentation, process control, computer peripherals, etc. An improved charge

For additional information, please refer to Application Note AN208 (FaxBack document #70606).

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE		
Logic	SW <sub>1</sub> , SW <sub>4</sub>	SW <sub>2</sub> , SW <sub>3</sub>
0	OFF	ON
1	ON	OFF

Logic "0"  $\leq 0.8\ \text{V}$   
 Logic "1"  $\geq 2.4\ \text{V}$

ORDERING INFORMATION		
Temp Range	Package	Part Number
-40 to 85°C	16-Pin Plastic DIP	DG213DJ
	16-Pin Narrow SOIC	DG213DY
	16-Pin TSSOP	DG213DQ



### ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-

V+ .....	44 V
GND .....	25 V
Digital Inputs <sup>a</sup> V <sub>S</sub> , V <sub>D</sub> .....	(V-) -2 V to (V+) +2 V or 30 mA, whichever occurs first
Current, Any Terminal .....	30 mA
Peak Current, S or D (Pulsed at 1 ms, 10% duty cycle max) .....	100 mA
Storage Temperature .....	-65 to 125°C

Power Dissipation (Package)<sup>b</sup>

16-Pin Plastic DIP <sup>c</sup> .....	470 mW
16-Pin Narrow SOIC <sup>d</sup> .....	640 mW
16-Pin TSSOP <sup>d</sup> .....	500 mW

- Notes:
- Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
  - All leads welded or soldered to PC Board.
  - Derate 6.5 mW/°C above 75°C
  - Derate 7.6 mW/°C above 75°C

SPECIFICATIONS							
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = -15 V V <sub>L</sub> = 5 V, V <sub>IN</sub> = 2.4 V, 0.8 V <sup>e</sup>	Temp <sup>a</sup>	D Suffix -40 to 85°C			Unit
				Min <sup>c</sup>	Typ <sup>b</sup>	Max <sup>c</sup>	
<b>Analog Switch</b>							
Analog Signal Range <sup>d</sup>	V <sub>ANALOG</sub>		Full	V-		V+	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	V <sub>D</sub> = ±10 V, I <sub>S</sub> = 1 mA	Room		45	60	Ω
r <sub>DS(on)</sub> Match	Δr <sub>DS(on)</sub>		Room		1	2	
Source Off Leakage Current	I <sub>S(off)</sub>	V <sub>S</sub> = ±14 V, V <sub>D</sub> = ∓14 V	Room	-0.5	±0.01	0.5	nA
Drain Off Leakage Current	I <sub>D(off)</sub>	V <sub>D</sub> = ±14 V, V <sub>S</sub> = ∓14 V	Room	-0.5	±0.01	0.5	
Drain On Leakage Current	I <sub>D(on)</sub>	V <sub>S</sub> = V <sub>D</sub> = 14 V	Room	-0.5	±0.02	0.5	
<b>Digital Control</b>							
Input Voltage High	V <sub>INH</sub>		Full	2.4			V
Input Voltage Low	V <sub>INL</sub>		Full			0.8	
Input Current	I <sub>INH</sub> or I <sub>INL</sub>	V <sub>INH</sub> or V <sub>INL</sub>	Full	-1		1	μA
Input Capacitance	C <sub>IN</sub>		Room		5		pF
<b>Dynamic Characteristics</b>							
Turn-On Time	t <sub>ON</sub>	V <sub>S</sub> = 10 V See Figure 2	Room		85	130	ns
Turn-Off Time	t <sub>OFF</sub>		Room		55	100	
Break-Before-Make Time Delay	t <sub>D</sub>	V <sub>S</sub> = 10 V, See Figure 3	Room	15	25		
Charge Injection	Q	C <sub>L</sub> = 1000 pF, V <sub>g</sub> = 0 V, R <sub>g</sub> = 0 Ω	Room		1		pC
Source-Off Capacitance	C <sub>S(off)</sub>	V <sub>S</sub> = 0 V, f = 1 MHz	Room		5		pF
Drain-Off Capacitance	C <sub>D(off)</sub>		Room		5		
Channel On Capacitance	C <sub>D(on)</sub>	V <sub>D</sub> = V <sub>S</sub> = 0 V, f = 1 MHz	Room		16		
Off Isolation	OIRR	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 50 Ω V <sub>S</sub> = 1 V <sub>RMS</sub> , f = 100 kHz	Room		90		dB
Channel-to-Channel Crosstalk	X <sub>TALK</sub>		Room		95		



SPECIFICATIONS							
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}$ , $V_- = -15\text{ V}$ $V_L = 5\text{ V}$ , $V_{IN} = 2.4\text{ V}$ , $0.8\text{ V}^e$	Temp <sup>a</sup>	D Suffix -40 to 85°C			Unit
				Min <sup>c</sup>	Typ <sup>b</sup>	Max <sup>c</sup>	
<b>Power Supply</b>							
Positive Supply Current	I+	$V_{IN} = 0\text{ or }5\text{ V}$	Room Full			1 5	$\mu\text{A}$
Negative Supply Current	I-		Room Full	-1 -5			
Logic Supply Current	I <sub>L</sub>		Room Full			1 5	
Power Supply Range for Continuous Operation	V <sub>OP</sub>		Full	±3		±22	V

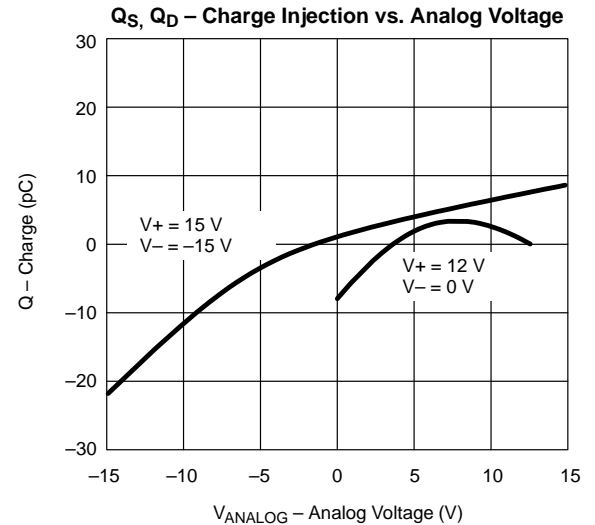
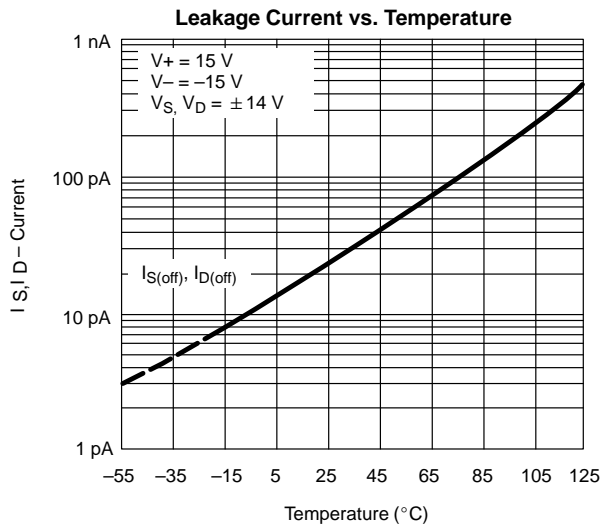
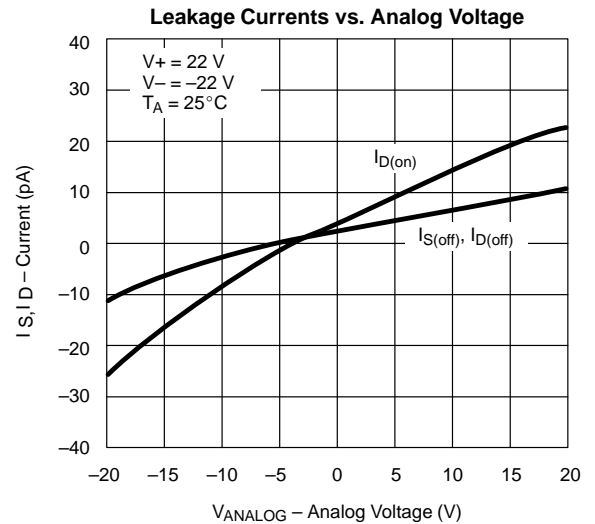
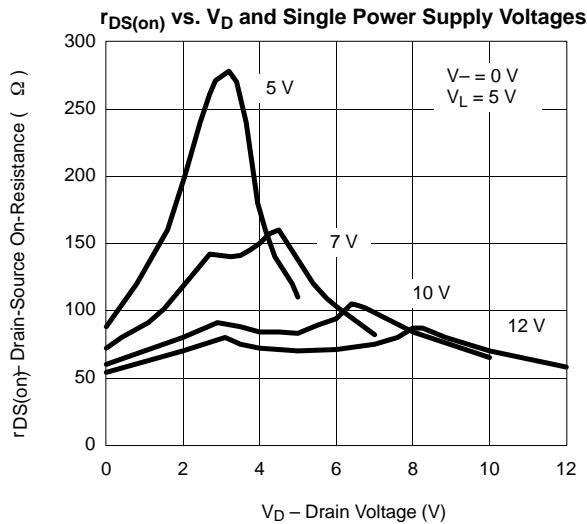
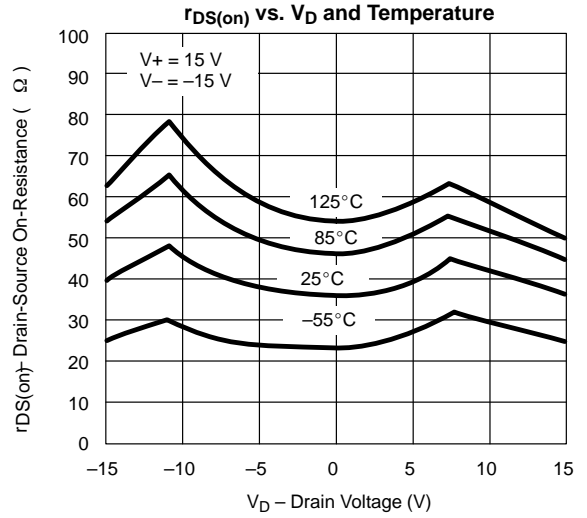
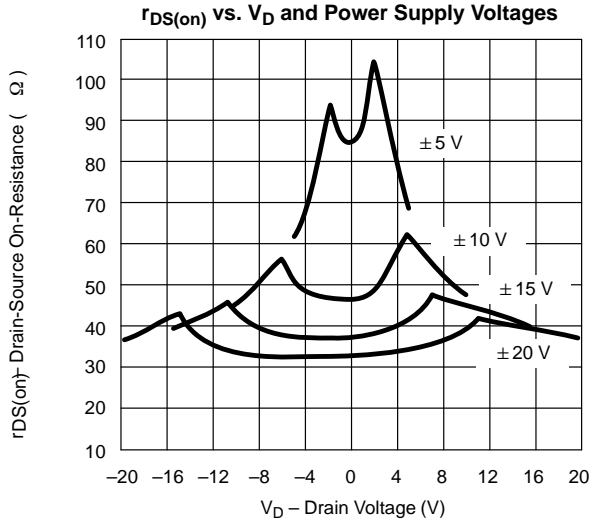
SPECIFICATIONS FOR UNIPOLAR SUPPLY							
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 12\text{ V}$ , $V_- = 0\text{ V}$ $V_L = 5\text{ V}$ , $V_{IN} = 2.4\text{ V}$ , $0.8\text{ V}^e$	Temp <sup>a</sup>	D Suffix -40 to 85°C			Unit
				Min <sup>c</sup>	Typ <sup>b</sup>	Max <sup>c</sup>	
<b>Analog Switch</b>							
Analog Signal Range <sup>d</sup>	V <sub>ANALOG</sub>		Full	V-		V+	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	$V_D = 3\text{ V}$ , $8\text{ V}$ , $I_S = 1\text{ mA}$	Room Full		90	110 140	$\Omega$
<b>Dynamic Characteristics</b>							
Turn-On Time	t <sub>ON</sub>	See Figure 2	Room		125	200	ns
Turn-Off Time	t <sub>OFF</sub>		Room		45	100	
Break-Before-Make Time Delay	t <sub>D</sub>	$V_S = 8\text{ V}$ , See Figure 3	Room	50	80		
Charge Injection	Q	$C_L = 1\text{ nF}$ , $V_{gen} = 6\text{ V}$ , $R_{gen} = 0\ \Omega$	Room		4		pC
<b>Power Supply</b>							
Positive Supply Current	I+	$V_{IN} = 0\text{ or }5\text{ V}$	Room Full			1 5	$\mu\text{A}$
Negative Supply Current	I-		Room Full	-1 -5			
Logic Supply Current	I <sub>L</sub>		Room Full			1 5	
Power Supply Range for Continuous Operation	V <sub>OP</sub>		Full	+3		+40	V

Notes:

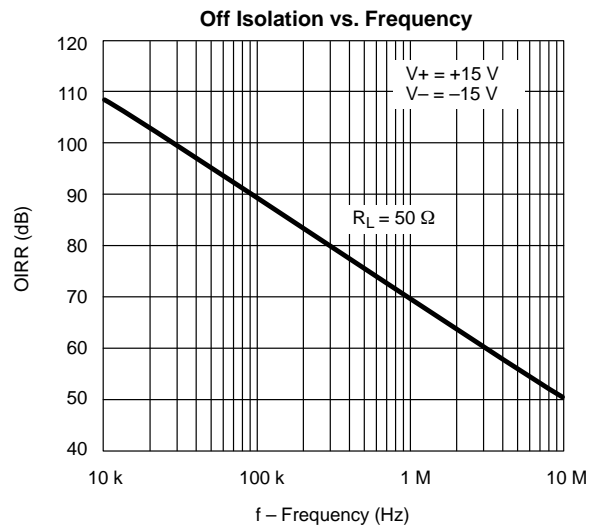
- a. Room = 25°C, Full = as determined by the operating temperature suffix.
- b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- d. Guaranteed by design, not subject to production test.
- e. V<sub>IN</sub> = input voltage to perform proper function.



**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**



**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**



**SCHEMATIC DIAGRAM (TYPICAL CHANNEL)**

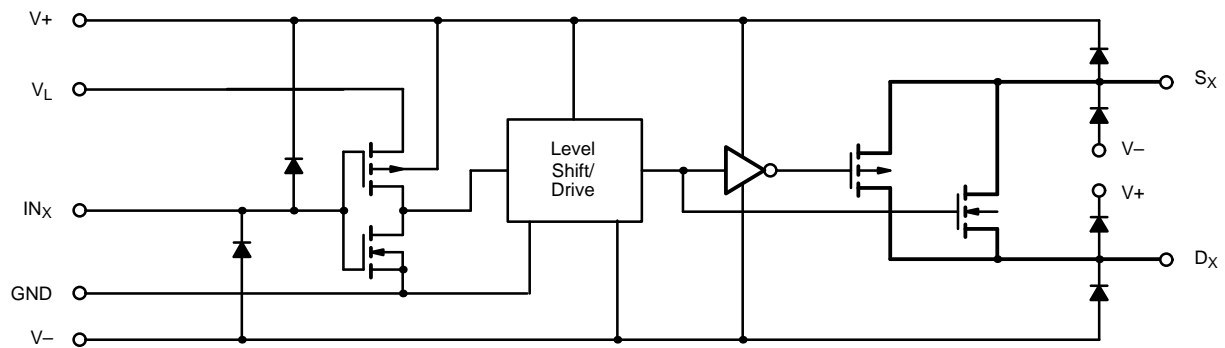


FIGURE 1.

**TEST CIRCUITS**

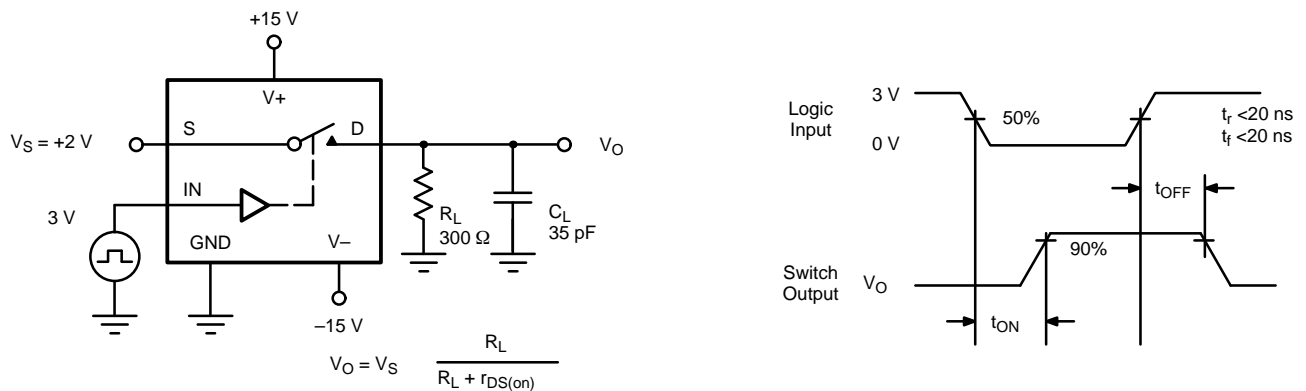
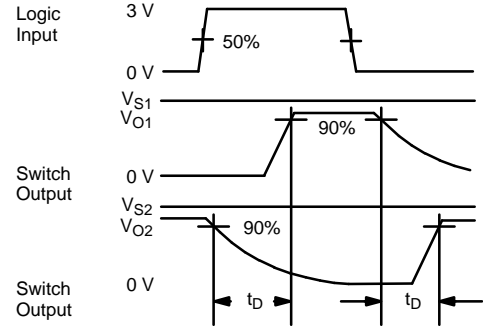
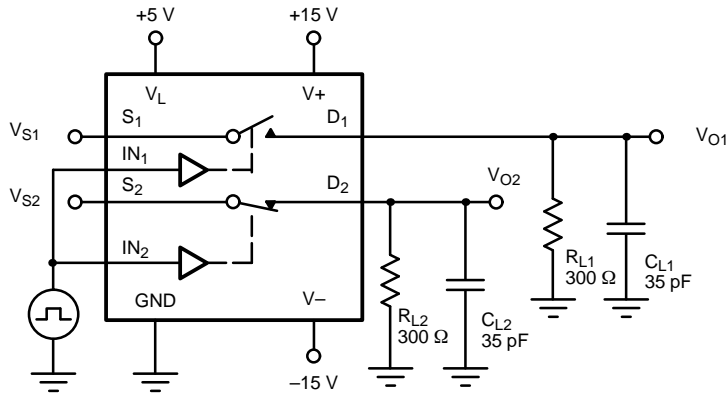


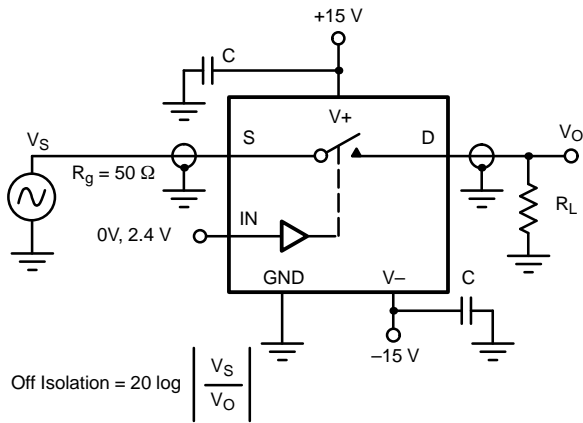
FIGURE 2. Switching Time

**TEST CIRCUITS**



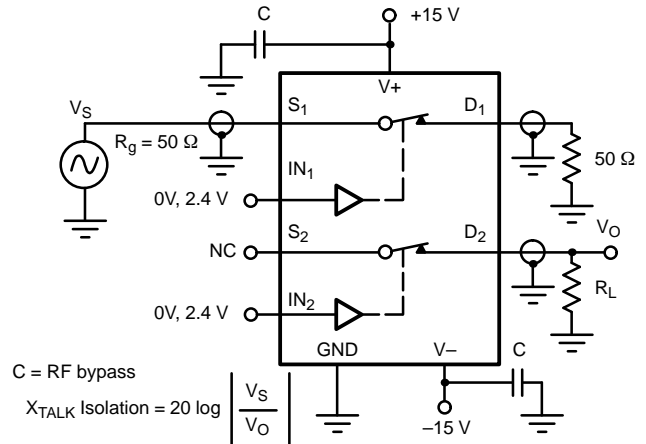
$C_L$  (includes fixture and stray capacitance)

**FIGURE 3. Break-Before-Make**



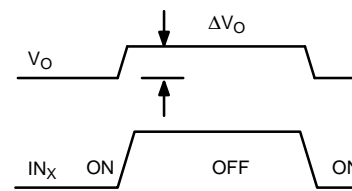
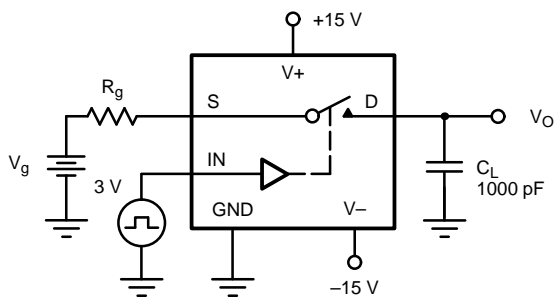
$$\text{Off Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

**FIGURE 4. Off Isolation**



$C = \text{RF bypass}$   
 $X_{\text{TALK}} \text{ Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$

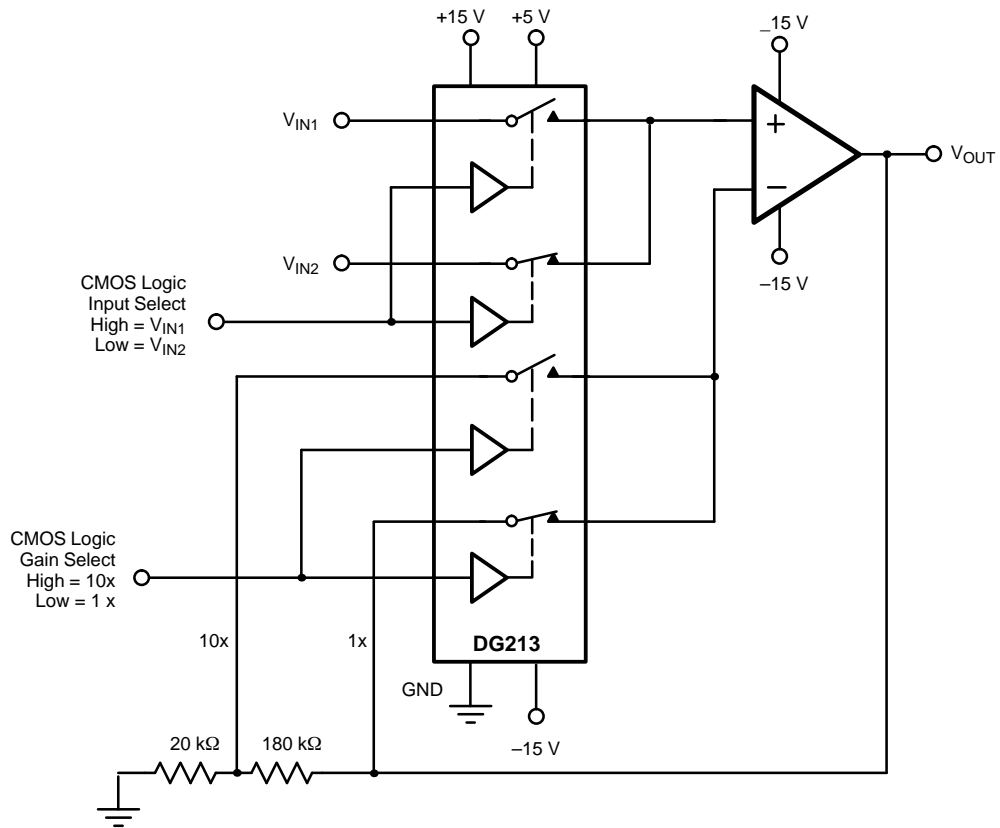
**FIGURE 5. Channel-to-Channel Crosstalk**



$\Delta V_O$  = measured voltage error due to charge injection  
 The charge injection in coulombs is  $Q = C_L \times \Delta V_O$

**FIGURE 6. Charge Injection**

**APPLICATIONS**



**FIGURE 7.** Low Power Non-Inverting Amplifier with Digitally Selectable Inputs and Gain



## Disclaimer

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