

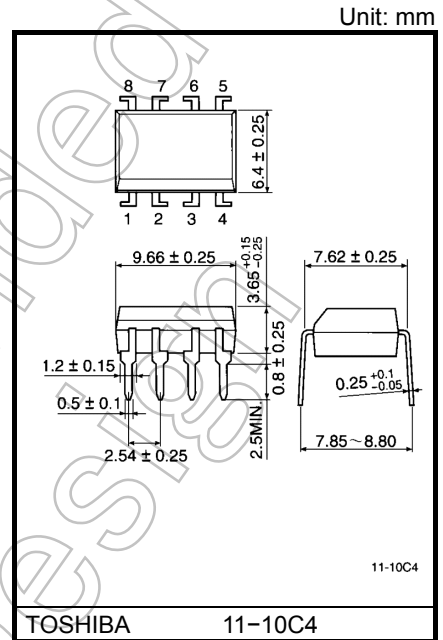
# TLP2630

Digital Logic Isolation  
 Tele-Communication  
 Analog Data Equipment Control  
 Microprocessor System Interface

The TOSHIBA TLP2630 dual photocoupler consists of a pair of GaAlAs light emitting diode and integrated high gain, high speed photodetector.

The output of the detector circuit is an open collector, Schottky clamped transistor. This unit is 8-lead DIP.

- Input current threshold:  $I_F = 5 \text{ mA}$  (max)
- LSTTL/TTL compatible: 5 V supply
- Switching speed: 10MBd (typ.)
- Guaranteed performance over temperature: 0 to 70°C
- Isolation voltage: 2500  $V_{rms}$  (min)
- UL recognized: UL1577, file no. E67349



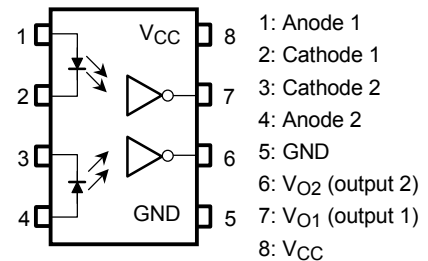
Weight: 0.54 g (typ.)

## Truth Table (positive logic)

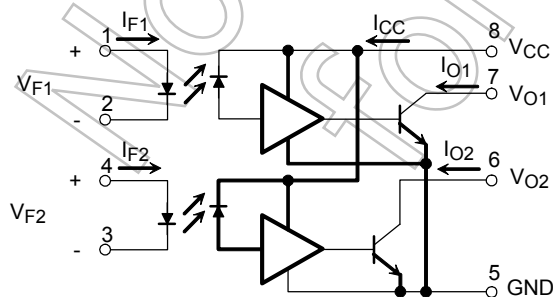
Input	Output
H	L
L	H

A 0.01 to 0.1μF bypass capacitor must be connected between pins 8 and 5 (see Note 1).

## Pin Configuration (top view)



## Schematic



Start of commercial production  
 1986/03

**Absolute Maximum Ratings (no derating required up to 70°C)**

Characteristic		Symbol	Rating	Unit
LED	Forward current(each channel)	I <sub>F</sub>	20	mA
	Pulse forward current (each channel)*	I <sub>FP</sub>	30	mA
	Reverse voltage(each channel)	V <sub>R</sub>	5	V
Detector	Output current(each channel)	I <sub>O</sub>	16	mA
	Output voltage(each channel)	V <sub>O</sub>	-0.5 to 7	V
	Supply voltage (1 minute maximum)	V <sub>CC</sub>	7	V
	Output collector power dissipation(each channel)	P <sub>O</sub>	40	mW
Operating temperature range		T <sub>stg</sub>	-55 to 125	°C
Storage temperature range		T <sub>opr</sub>	-40 to 85	°C
Lead soldering temperature (10 s) (Note 1)		T <sub>sol</sub>	260	°C
Isolation voltage (AC, 1 minute, R.H.≤ 60%, Note 3)		BV <sub>S</sub>	2500	V <sub>rms</sub>

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

\* t ≤ 1 msec duration.

**Recommended Operating Conditions**

Characteristic	Symbol	Min	Typ.	Max	Unit
Input current, low level, each channel	I <sub>FL</sub>	0	—	250	μA
Input current, high level, each channel	I <sub>FH</sub>	6.3*	—	15	mA
Supply voltage**, output	V <sub>CC</sub>	4.5	5	5.5	V
Fan out(TTL load, each channel)	N	—	—	8	
Operating temperature	T <sub>opr</sub>	0	—	70	°C

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

\* 6.3mA is a guard banded value which allows for at least 20% CTR degradation. Initial input current threshold value is 5.0mA or less.

\*\*This item denotes operating ranges, not meaning of recommended operating conditions.

## Electrical Characteristics (Ta = 0~70°C, unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ.*	Max	Unit
Input forward voltage (each channel)	V <sub>F</sub>	I <sub>F</sub> = 10mA, Ta = 25°C	—	1.65	1.75	V
Input diode temperature coefficient(each channel)	ΔV <sub>F</sub> / ΔTa	I <sub>F</sub> = 10mA	—	-2.0	—	mV / °C
Input reverse breakdown voltage(each channel)	BV <sub>R</sub>	I <sub>R</sub> = 10μA, Ta = 25°C	5	—	—	V
Input capacitance (each channel)	C <sub>T</sub>	V <sub>F</sub> = 0, f = 1MHz	—	45	—	pF
High level output current (each channel)	I <sub>OH</sub>	V <sub>CC</sub> = 5.5V, V <sub>O</sub> = 5.5V I <sub>F</sub> = 250μA	—	1	250	μA
Low level output voltage (each channel)	V <sub>OL</sub>	V <sub>CC</sub> = 5.5V, I <sub>F</sub> = 5mA I <sub>OL</sub> (sinking) = 13mA	—	0.4	0.6	V
High level supply current (both channels)	I <sub>CCH</sub>	V <sub>CC</sub> = 5.5V, I <sub>F</sub> = 0	—	14	30	mA
Low level supply current (both channels)	I <sub>CCL</sub>	V <sub>CC</sub> = 5.5V, I <sub>F</sub> = 10mA	—	24	36	mA
Isolation resistance	R <sub>S</sub>	V <sub>S</sub> = 500V, R.H. ≤ 60% (Note 3)	—	10 <sup>14</sup>	—	Ω
Capacitance (input-output)	C <sub>S</sub>	f = 1MHz (Note 3)	—	0.6	—	pF
Input-input leakage current	I <sub>I-I</sub>	R.H. ≤ 60%, t = 5s V <sub>I-I</sub> = 500V (Note 6)	—	0.005	—	μA
Resistance (input-input)	R <sub>I-I</sub>	V <sub>I-I</sub> = 500V (Note 6)	—	10 <sup>11</sup>	—	Ω
Capacitance (input-input)	C <sub>I-I</sub>	f = 1MHz (Note 6)	—	0.25	—	pF

\* All typical values are at V<sub>CC</sub> = 5V, Ta = 25°C.

**Switching Characteristics (Ta =25°C , VCC=5V)**

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time to low output level	$t_{pHL}$	1	$I_F = 0 \rightarrow 7.5mA, R_L = 350\Omega$ $C_L = 15pF$ (each channel)	—	60	75	ns
Propagation delay time to high output level	$t_{pLH}$	1	$I_F = 7.5mA \rightarrow 0, R_L = 350\Omega$ $C_L = 15pF$ (each channel)	—	60	75	ns
Output rise a time,output fall time(10~90%)	$t_r, t_f$	1	$I_F = 0 \leftrightarrow 7.5mA, R_L = 350\Omega$ $C_L = 15pF$ (each channel)	—	30	—	ns
Common mode transient immunity at high output level	$CM_H$	2	$I_F = 0, R_L = 350\Omega$ $V_{CM} = 200V$ $V_{O(min)} = 2V$ (each channel, Note 4)	—	200	—	V / $\mu s$
Common mode transient immunity at low output level	$CM_L$	2	$I_F = 7.5mA, R_L = 350\Omega$ $V_{CM} = 200V$ $V_{O(max)} = 0.8V$ (each channel, Note 5)	—	500	—	V / $\mu s$

(Note 1) 2mm below seating plane.

(Note 2) The  $V_{CC}$  supply voltage to each TLP2630 isolator must be bypassed by a 0.01 $\mu F$  capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package  $V_{CC}$  and GND pins each device.

(Note 3) Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

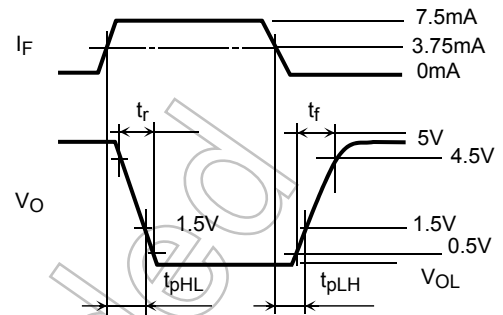
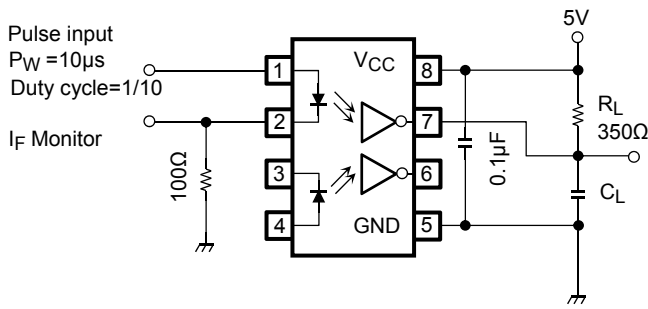
(Note 4)  $CM_H$  the maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the high state(i.e.  $V_{OUT} > 2.0V$ )

(Note 5)  $CM_L$  the maximum tolerable rate of fall of the common mode voltage to ensure the output will remain in the low output state(i.e.  $V_{OUT} < 0.8V$ ) Measured in volts per microsecond(V /  $\mu s$ ).

(Note 6) Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.

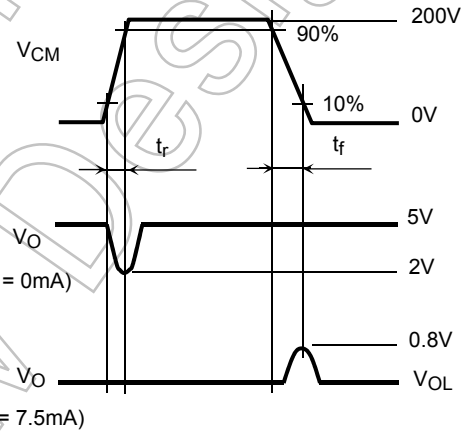
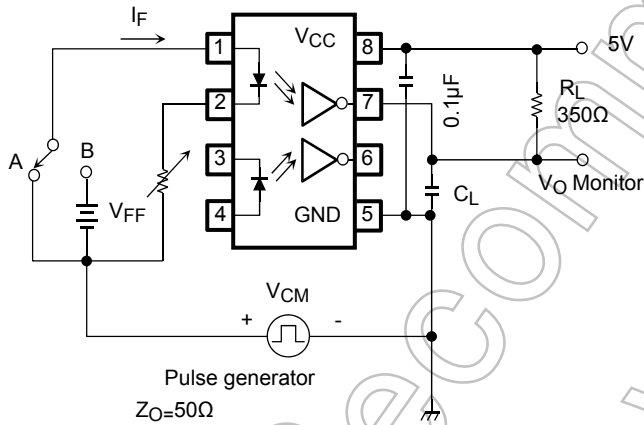
Not Recommended for New

**Test Circuit 1.  $t_{pHL}$  and  $t_{pLH}$**



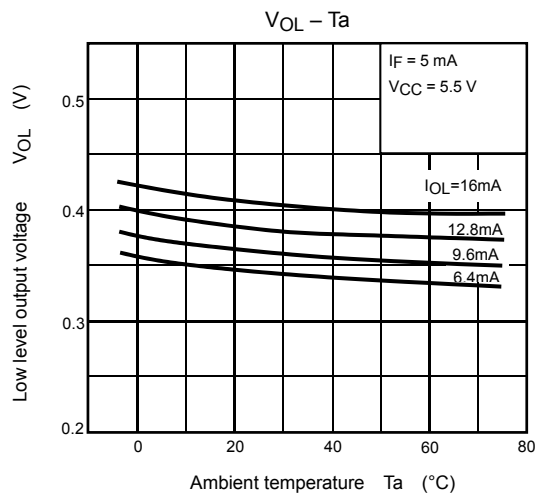
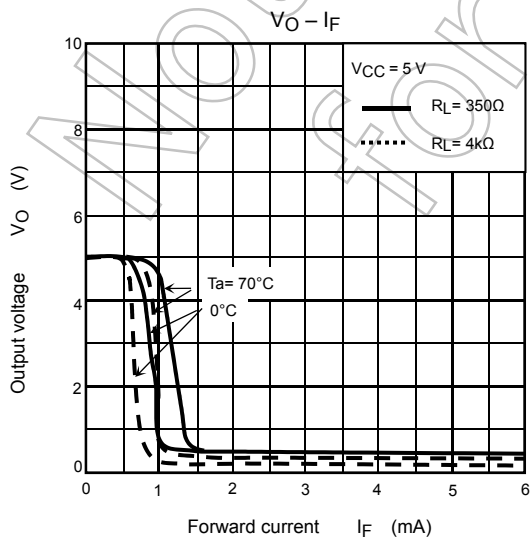
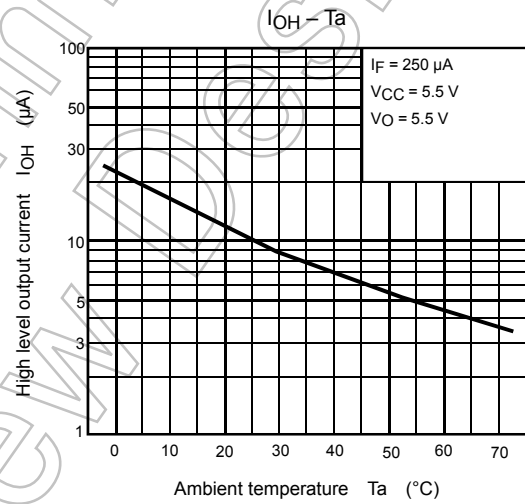
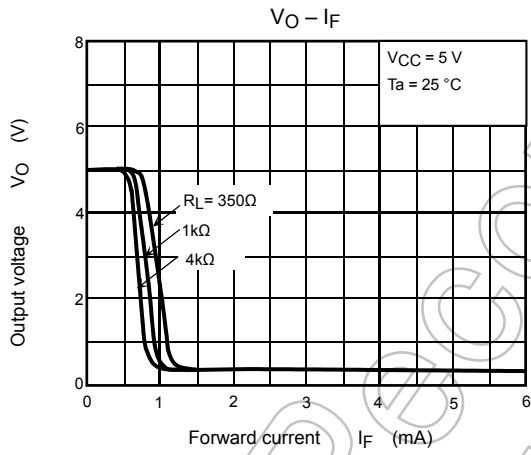
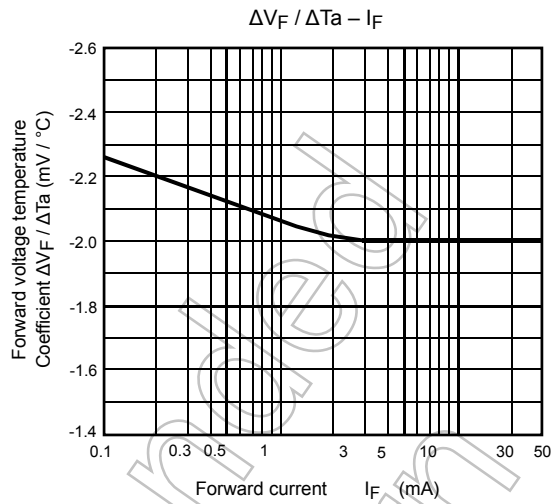
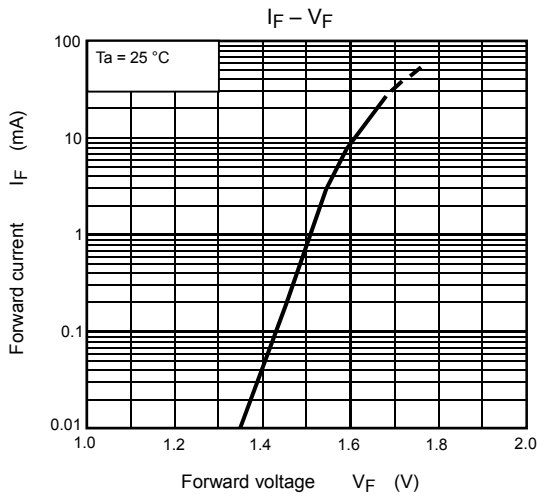
\*  $C_L$  is approximately 15pF which includes probe and stray wiring capacitance.

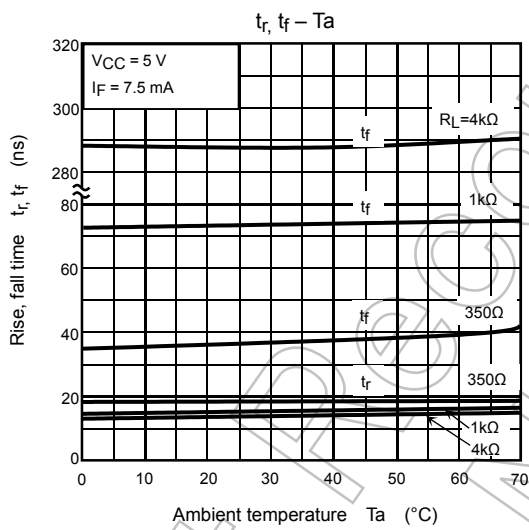
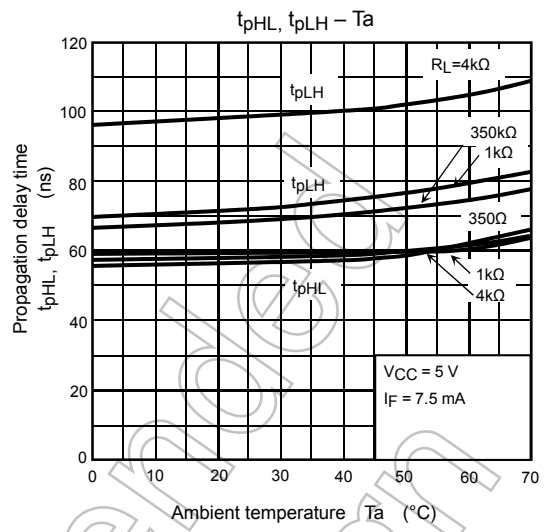
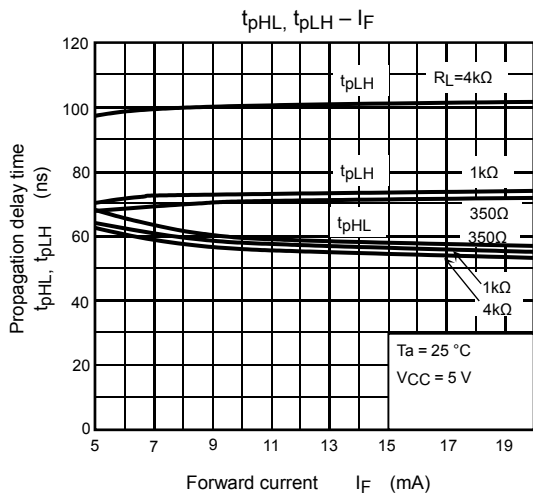
**Test Circuit 2. Transient Immunity and Typical Waveforms**



$$CM_H = \frac{160(V)}{t_r(\mu s)}, CM_L = \frac{160(V)}{t_f(\mu s)}$$

\*  $C_L$  is approximately 15pF which includes probe and stray wiring capacitance.





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