

# TK13E25D

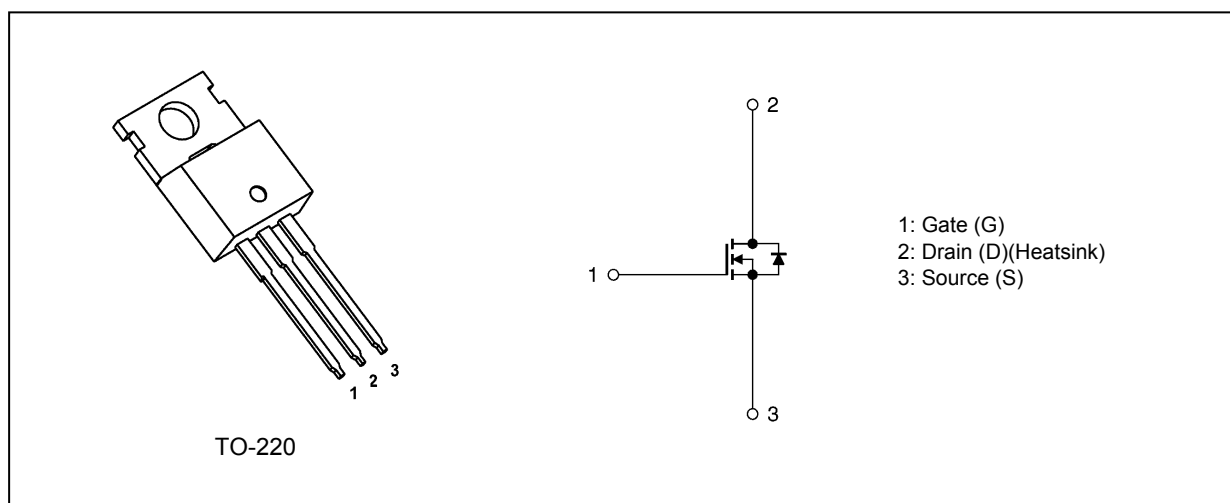
## 1. Applications

- Switching Voltage Regulators

## 2. Features

- (1) Low drain-source on-resistance:  $R_{DS(ON)} = 0.19 \Omega$  (typ.)
- (2) Low leakage current:  $I_{DSS} = 10 \mu A$  (max) ( $V_{DS} = 250 V$ )
- (3) Enhancement mode:  $V_{th} = 1.5$  to  $3.5 V$  ( $V_{DS} = 10 V, I_D = 1 mA$ )

## 3. Packaging and Internal Circuit



## 4. Absolute Maximum Ratings (Note) ( $T_a = 25^\circ C$ unless otherwise specified)

| Characteristics                          | Symbol    | Rating     | Unit       |
|--|-----------|------------|------------|
| Drain-source voltage                     | $V_{DSS}$ | 250        | V          |
| Gate-source voltage                      | $V_{GSS}$ | $\pm 20$   |            |
| Drain current (DC) (Note 1)              | $I_D$     | 13         | A          |
| Drain current (pulsed) (Note 1)          | $I_{DP}$  | 52         |            |
| Power dissipation ( $T_c = 25^\circ C$ ) | $P_D$     | 102        | W          |
| Single-pulse avalanche energy (Note 2)   | $E_{AS}$  | 78         | mJ         |
| Avalanche current (Note 3)               | $I_{AR}$  | 13         | A          |
| Reverse drain current (DC) (Note 1)      | $I_{DR}$  | 13         |            |
| Reverse drain current (pulsed) (Note 1)  | $I_{DRP}$ | 52         |            |
| Channel temperature                      | $T_{ch}$  | 150        | $^\circ C$ |
| Storage temperature                      | $T_{stg}$ | -55 to 150 |            |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Start of commercial production

2010-11

**5. Thermal Characteristics**

| Characteristics                       | Symbol         | Max  | Unit |
|---------------------------------------|----------------|------|------|
| Channel-to-case thermal resistance    | $R_{th(ch-c)}$ | 1.23 | °C/W |
| Channel-to-ambient thermal resistance | $R_{th(ch-a)}$ | 83.3 |      |

Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2:  $V_{DD} = 50\text{ V}$ ,  $T_{ch} = 25^\circ\text{C}$  (initial),  $L = 0.77\text{ mH}$ ,  $R_G = 25\ \Omega$ ,  $I_{AR} = 13\text{ A}$

Note 3: Repetitive rating; pulse width limited by maximum channel temperature

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

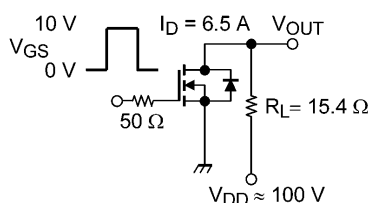
**6. Electrical Characteristics**

**6.1. Static Characteristics ( $T_a = 25^\circ\text{C}$  unless otherwise specified)**

| Characteristics                | Symbol        | Test Condition                                  | Min | Typ. | Max     | Unit          |
|--------------------------------|---------------|---|-----|------|---------|---------------|
| Gate leakage current           | $I_{GSS}$     | $V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$ | —   | —    | $\pm 1$ | $\mu\text{A}$ |
| Drain cut-off current          | $I_{DSS}$     | $V_{DS} = 250\text{ V}, V_{GS} = 0\text{ V}$    | —   | —    | 10      |               |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | $I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$       | 250 | —    | —       | V             |
| Gate threshold voltage         | $V_{th}$      | $V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$       | 1.5 | —    | 3.5     |               |
| Drain-source on-resistance     | $R_{DS(ON)}$  | $V_{GS} = 10\text{ V}, I_D = 6.5\text{ A}$      | —   | 0.19 | 0.25    | $\Omega$      |

**6.2. Dynamic Characteristics ( $T_a = 25^\circ\text{C}$  unless otherwise specified)**

| Characteristics                | Symbol    | Test Condition   | Min | Typ. | Max | Unit        |
|--------------------------------|-----------|--|-----|------|-----|-------------|
| Input capacitance              | $C_{iss}$ | $V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$ | —   | 1100 | —   | $\text{pF}$ |
| Reverse transfer capacitance   | $C_{rss}$ |  | —   | 8    | —   |             |
| Output capacitance             | $C_{oss}$ |  | —   | 66   | —   |             |
| Gate resistance                | $r_g$     | $V_{DS} = \text{OPEN}, f = 1\text{ MHz}$                       | —   | 5    | —   | $\Omega$    |
| Switching time (rise time)     | $t_r$     | See Figure 6.2.1.  | —   | 40   | —   | ns          |
| Switching time (turn-on time)  | $t_{on}$  |  | —   | 55   | —   |             |
| Switching time (fall time)     | $t_f$     |  | —   | 20   | —   |             |
| Switching time (turn-off time) | $t_{off}$ |  | —   | 130  | —   |             |



Duty  $\leq 1\%$ ,  $t_w = 10\ \mu\text{s}$

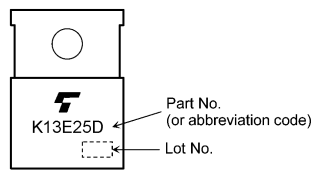
**Fig. 6.2.1 Switching Time Test Circuit**

**6.3. Gate Charge Characteristics ( $T_a = 25^\circ\text{C}$  unless otherwise specified)**

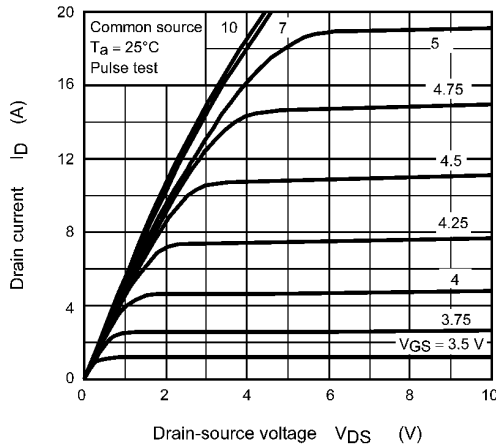
| Characteristics                                 | Symbol    | Test Condition   | Min | Typ. | Max | Unit |
|---|-----------|--|-----|------|-----|------|
| Total gate charge (gate-source plus gate-drain) | $Q_g$     | $V_{DD} \approx 200\text{ V}, V_{GS} = 10\text{ V}, I_D = 13\text{ A}$ | —   | 25   | —   | nC   |
| Gate-source charge 1                            | $Q_{gs1}$ |  | —   | 4.2  | —   |      |
| Gate-drain charge                               | $Q_{gd}$  |  | —   | 8.5  | —   |      |

**6.4. Source-Drain Characteristics ( $T_a = 25^\circ\text{C}$  unless otherwise specified)**

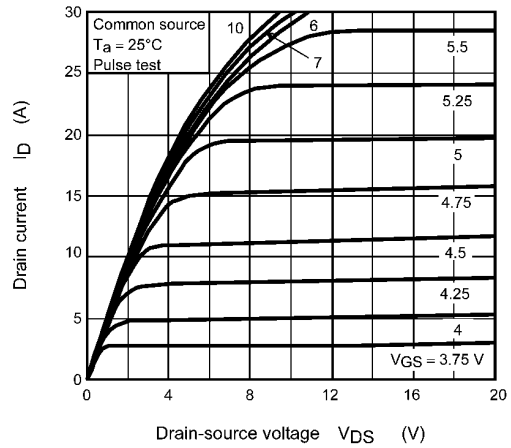
| Characteristics               | Symbol    | Test Condition  | Min | Typ. | Max  | Unit          |
|-------------------------------|-----------|---|-----|------|------|---------------|
| Diode forward voltage         | $V_{DSF}$ | $I_{DR} = 13\text{ A}, V_{GS} = 0\text{ V}$   | —   | —    | -1.7 | V             |
| Reverse recovery time         | $t_{rr}$  | $I_{DR} = 13\text{ A}, V_{GS} = 0\text{ V}$<br>$-di_{DR}/dt = 100\text{ A}/\mu\text{s}$ | —   | 180  | —    | ns            |
| Reverse recovery charge       | $Q_{rr}$  |   | —   | 1.1  | —    | $\mu\text{C}$ |
| Peak reverse recovery current | $I_{rr}$  |   | —   | 12   | —    | A             |

**7. Marking****Fig. 7.1 Marking**

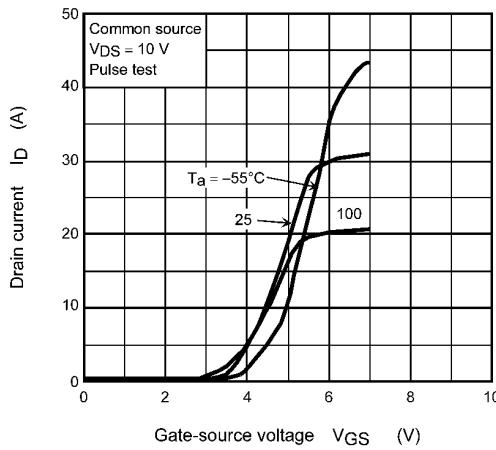
**8. Characteristics Curves (Note)**



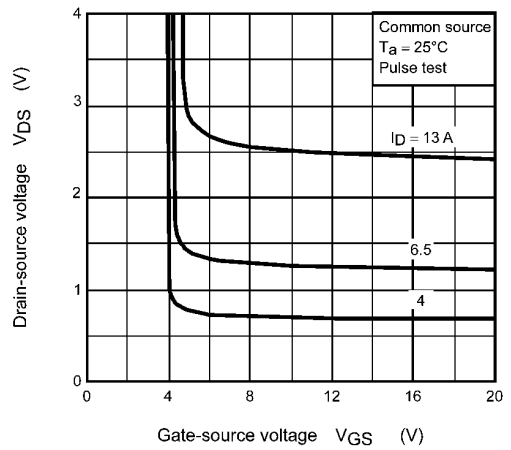
**Fig. 8.1  $I_D - V_{DS}$**



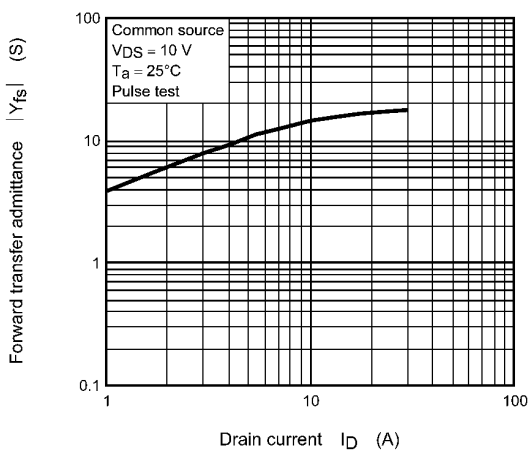
**Fig. 8.2  $I_D - V_{DS}$**



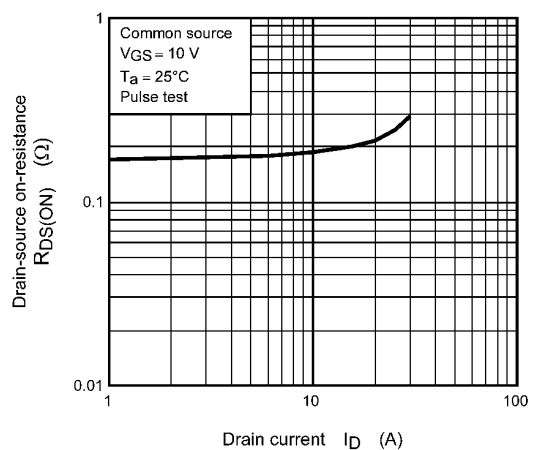
**Fig. 8.3  $I_D - V_{GS}$**



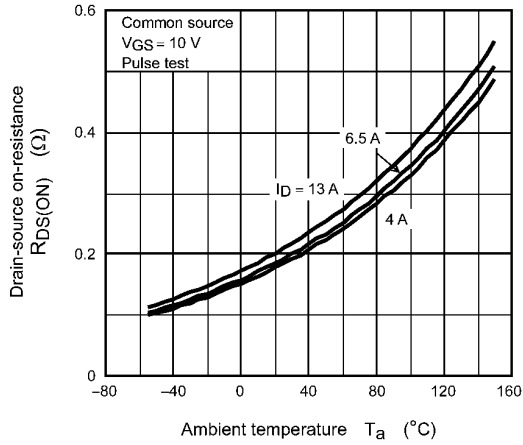
**Fig. 8.4  $V_{DS} - V_{GS}$**



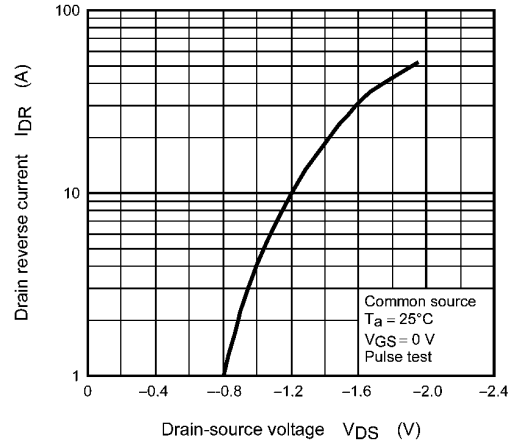
**Fig. 8.5  $|Y_{fs}| - I_D$**



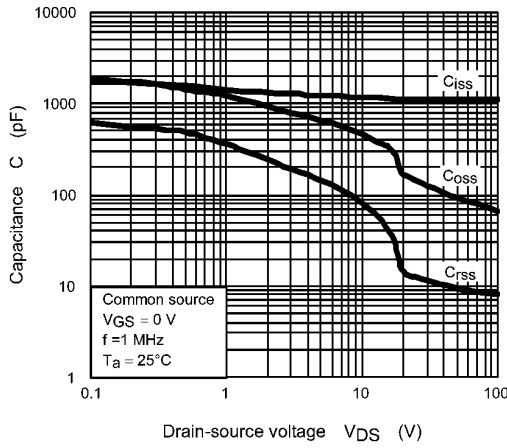
**Fig. 8.6  $R_{DS(ON)} - I_D$**



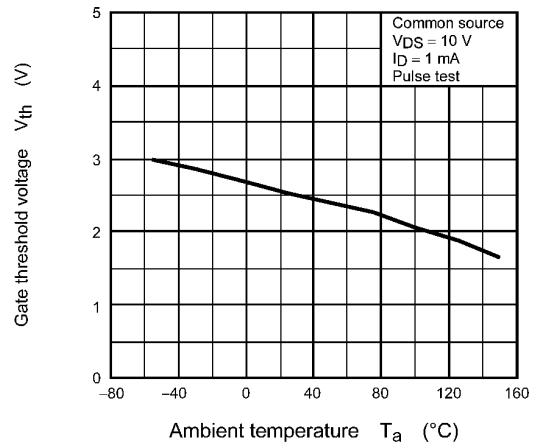
**Fig. 8.7  $R_{DS(ON)} - T_a$**



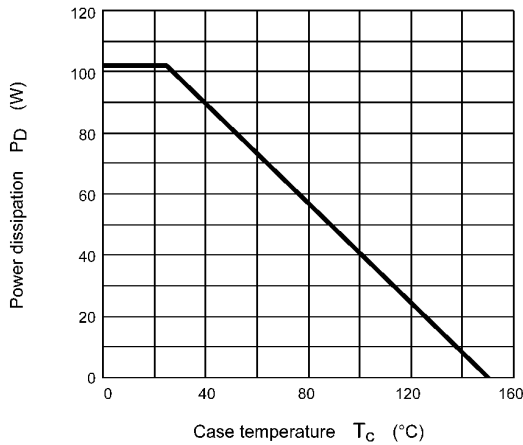
**Fig. 8.8  $I_{DR} - V_{DS}$**



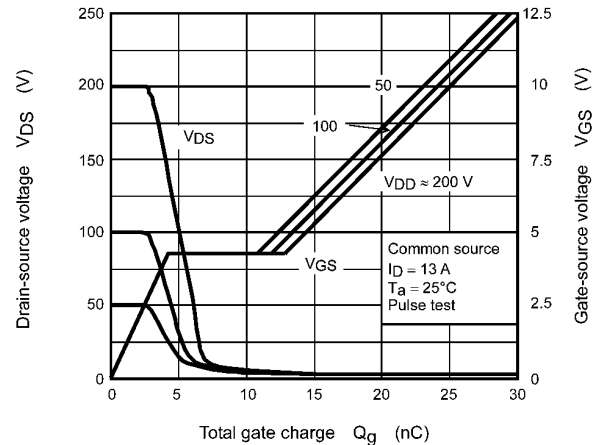
**Fig. 8.9  $C - V_{DS}$**



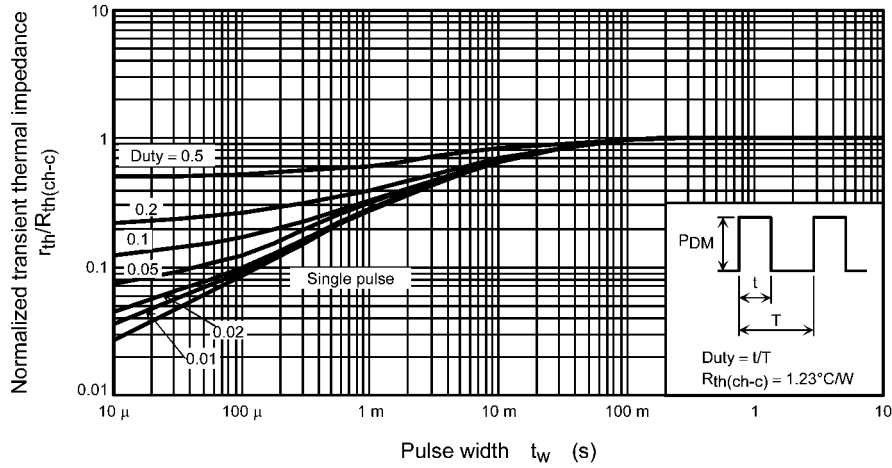
**Fig. 8.10  $V_{th} - T_a$**



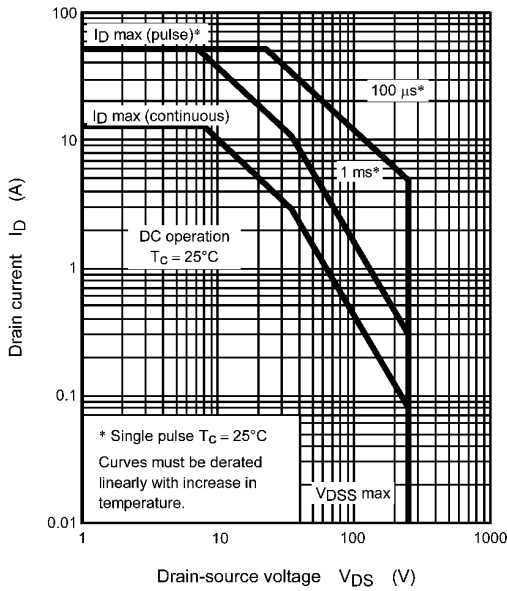
**Fig. 8.11  $P_D - T_c$   
(Guaranteed Maximum)**



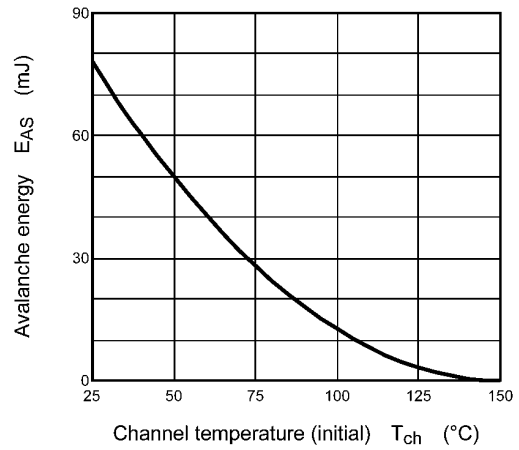
**Fig. 8.12 Dynamic Input/Output Characteristics**



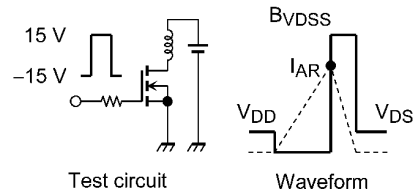
**Fig. 8.13**  $r_{th}/R_{th(ch-c)} - t_w$   
(Guaranteed Maximum)



**Fig. 8.14** Safe Operating Area  
(Guaranteed Maximum)



**Fig. 8.15**  $E_{AS} - T_{ch}$   
(Guaranteed Maximum)



$$R_G = 25 \Omega, V_{DD} = 50 \text{ V} \quad E_{AS} = \frac{1}{2} \cdot L \cdot I_{AR}^2 \cdot \left( \frac{BV_{DS}}{BV_{DS} - V_{DD}} \right)$$

**Fig. 8.16** Test Circuit/Waveform

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.





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