

# STK5Q4U362J-E

## Advance Information 10A/600V Integrated Power Module in Compact DIP package

The STK5Q4U362J-E is a fully-integrated inverter power stage consisting of a high-voltage driver, six IGBT's and a thermistor, suitable for driving permanent magnet synchronous (PMSM) motors, brushless-DC (BLDC) motors and AC asynchronous motors. The IGBT's are configured in a 3-phase bridge with separate emitter connections for the lower legs for maximum flexibility in the choice of control algorithm. The power stage has a full range of protection functions including cross-conduction protection, external shutdown and under-voltage lockout functions. An internal comparator and reference connected to the over-current protection circuit allows the designer to set the over-current protection level.

### Features

- Three-phase 10A/600V IGBT module with integrated drivers
- Typical values :  $V_{CE(SAT)} = 1.8V$ ,  $V_F = 1.5V$ ,  $E_{SW} = 390\mu J$  at 10A
- Compact 29.6mm x 18.2mm dual in-line package
- Cross-conduction protection
- Adjustable over-current protection level
- Integrated bootstrap diodes and resistors
- Enable pin
- Thermistor

### Typical Applications

- Industrial Pumps
- Industrial Fans
- Industrial Automation
- Home Appliances

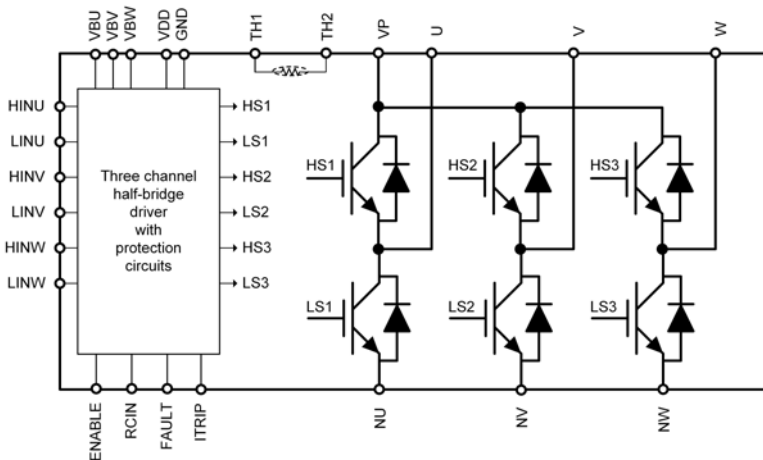


Figure 1. Functional Diagram

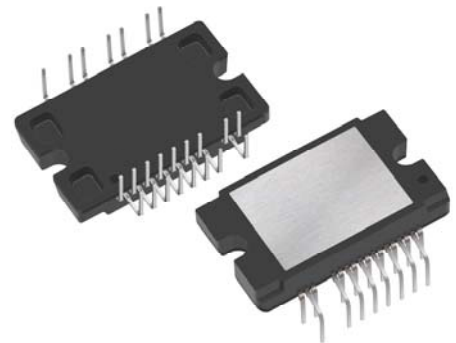
This document contains information on a new product. Specifications and information herein are subject to change without notice.



ON Semiconductor®

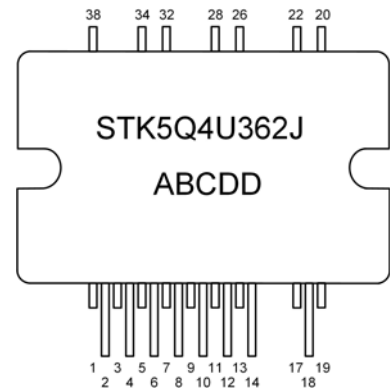
www.onsemi.com

### PACKAGE PICTURE



MODULE SPCM24 29.6x18.2 DIP S3

### MARKING DIAGRAM



STK5Q4U362J = Specific Device Code  
 A = Year  
 B = Month  
 C = Production Site  
 DD = Factory Lot Code  
 Device marking is on package underside

### ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
STK5Q4U362J-E	MODULE SPCM24 29.6x18.2 DIP S3 (Pb-Free)	16 / Tube

# STK5Q4U362J-E

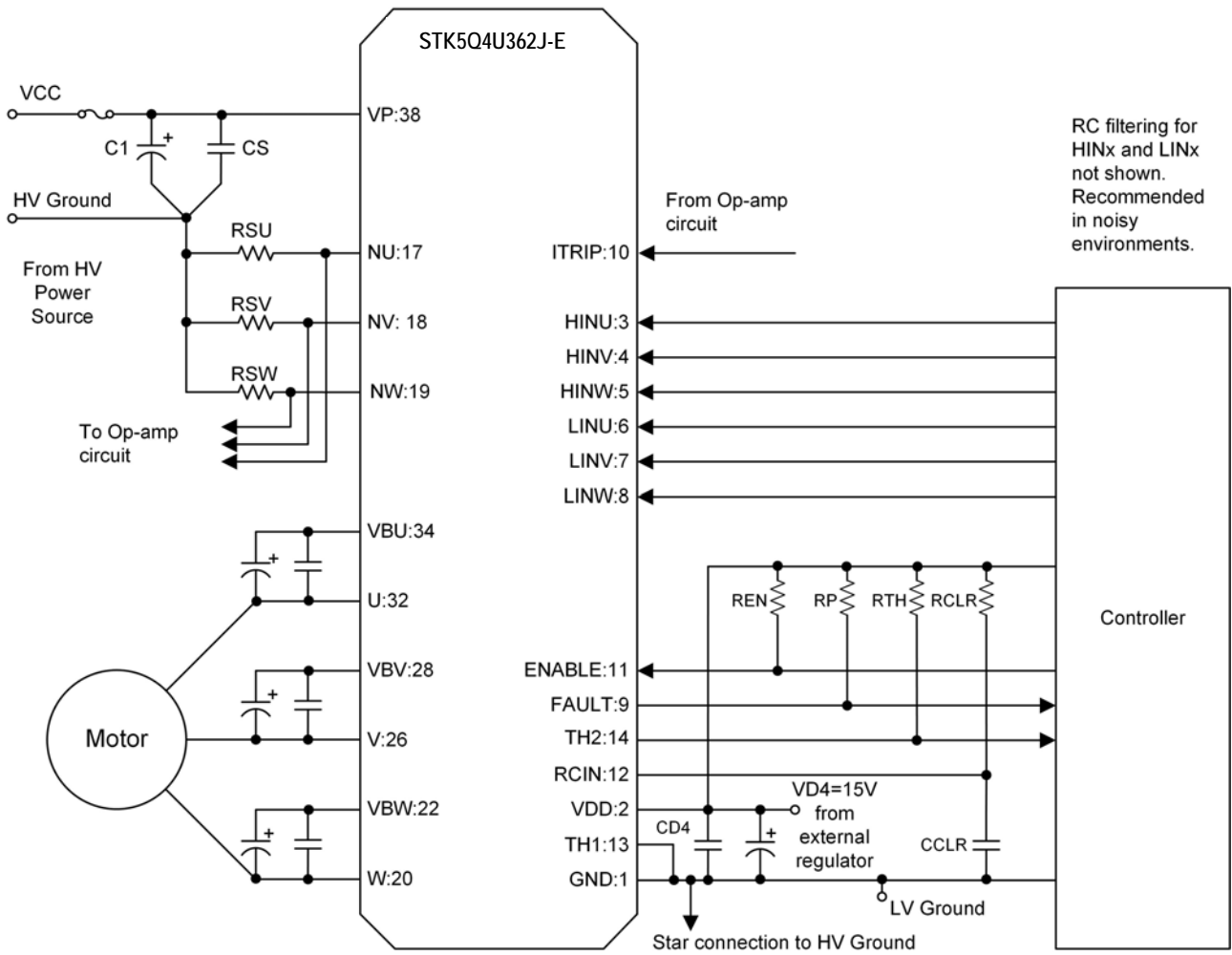


Figure 2. Application Schematic

# STK5Q4U362J-E

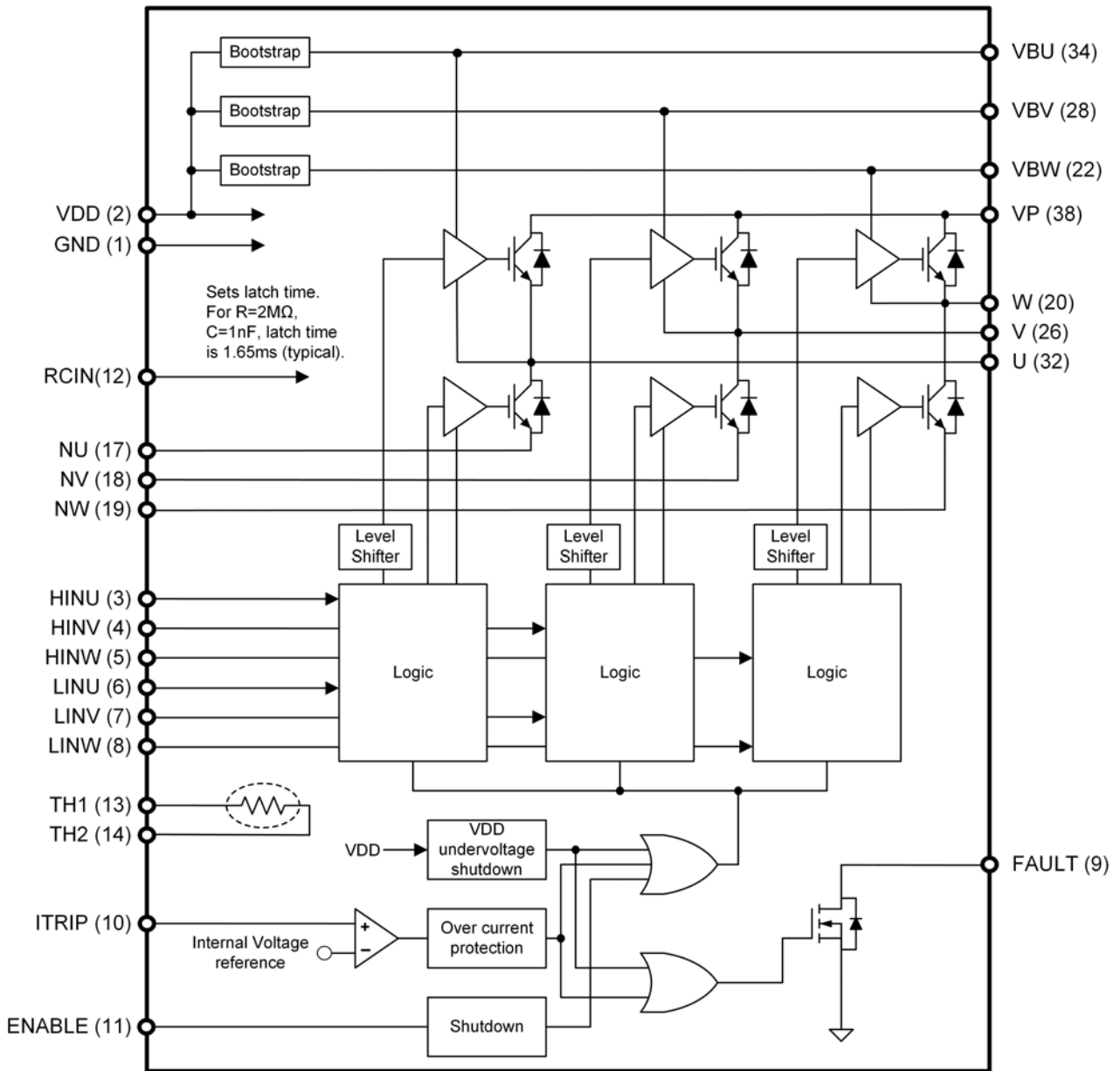


Figure 3. Simplified Block Diagram

# STK5Q4U362J-E

## PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	GND	Negative Main Supply
2	VDD	+15V Main Supply
3	HINU	Logic Input High Side Gate Driver - Phase U
4	HINV	Logic Input High Side Gate Driver - Phase V
5	HINW	Logic Input High Side Gate Driver - Phase W
6	LINU	Logic Input Low Side Gate Driver - Phase U
7	LINV	Logic Input Low Side Gate Driver - Phase V
8	LINW	Logic Input Low Side Gate Driver - Phase W
9	FAULT	Fault output
10	ITRIP	Current protection pin
11	ENABLE	Enable input
12	RCIN	R,C connection terminal for setting FAULT clear time
13	TH1	Thermistor output 1
14	TH2	Thermistor output 2
17	NU	Low Side Emitter Connection - Phase U
18	NV	Low Side Emitter Connection - Phase V
19	NW	Low Side Emitter Connection - Phase W
20	W	W phase output. Internally connected to W phase high side driver ground
22	VBW	High Side Floating Supply Voltage for W phase
26	V	V phase output. Internally connected to V phase high side driver ground
28	VBV	High Side Floating Supply voltage for V phase
32	U	U phase output. Internally connected to U phase high side driver ground
34	VBU	High Side Floating Supply voltage for U phase
38	VP	Positive Bus Input Voltage

Note: Pins 15, 16, 21, 23, 24, 25, 27, 29, 30, 31, 33, 35, 36, 37 are not present

## STK5Q4U362J-E

### ABSOLUTE MAXIMUM RATINGS (Notes 1,2)

Rating	Symbol	Conditions	Value	Unit
Supply voltage	$V_{CC}$	VP to NU, NV, NW, surge < 500V (Note 3)	450	V
Collector-emitter voltage	$V_{CE\ max}$	VP to U, V, W ; U to NU ; V to NV ; W to NW	600	V
Output current	$I_o$	VP, U, V, W, NU, NV, NW terminal current	$\pm 10$	A
		VP, U, V, W, NU, NV, NW terminal current, $T_c=100^\circ\text{C}$	$\pm 5$	A
Output peak current	$I_{op}$	VP, U, V, W, NU, NV, NW terminal current, pulse width 1ms	$\pm 20$	A
Gate driver supply voltages	$V_{DD}, V_{BS}$	VBU to U, VBV to V, VBW to W, $V_{DD}$ to GND (Note 4)	-0.3 to +20.0	V
Input signal voltage	$V_{IN}$	HINU, HINV, HINW, LINU, LINV, LINW	-0.3 to $V_{DD}$	V
FAULT terminal voltage	VFAULT	FAULT terminal	-0.3 to $V_{DD}$	V
RCIN terminal voltage	VRCIN	RCIN terminal	-0.3 to $V_{DD}$	V
ITRIP terminal voltage	VITRIP	ITRIP terminal	-0.3 to +10.0	V
ENABLE terminal voltage	VENABLE	ENABLE terminal	-0.3 to $V_{DD}$	V
Maximum power dissipation	$P_d$	IGBT per 1 channel	31	W
Junction temperature	$T_j$	IGBT, Gate driver IC	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-40 to +125	$^\circ\text{C}$
Operating case temperature	$T_c$	IPM case temperature	-20 to +100	$^\circ\text{C}$
Package mounting torque		Case mounting screw	0.6	Nm
Isolation voltage	Vis	50Hz sine wave AC 1 minute (Note 5)	2000	V <sub>rms</sub>

- Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
- Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
- This surge voltage developed by the switching operation due to the wiring inductance between VP and NU, NV, NW terminals.
- $V_{BS}=V_{BU}$  to U,  $V_{BV}$  to V,  $V_{BW}$  to W.
- Test conditions : AC2500V, 1 s

### RECOMMENDED OPERATING RANGES (Note 6)

Rating	Symbol		Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	VP to NU, NV, NW	0	280	400	V
Gate driver supply voltage	$V_{BS}$	VBU to U, VBV to V, VBW to W	12.5	15	17.5	V
	$V_{DD}$	$V_{DD}$ to GND (Note 4)	13.5	15	16.5	
ON-state input voltage	$V_{IN(ON)}$	HINU, HINV, HINW, LINU, LINV, LINW	3.0		5.0	V
OFF-state input voltage	$V_{IN(OFF)}$		0		0.3	
PWM frequency	fPWM		1		20	kHz
Dead time	DT	Turn-off to turn-on (external)	1			$\mu\text{s}$
Allowable input pulse width	PWIN	ON and OFF	1			$\mu\text{s}$
Package mounting torque		'M3' type screw	0.4		0.6	Nm

- Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# STK5Q4U362J-E

## ELECTRICAL CHARACTERISTICS

at Tc=25°C, VBS=15V, VDD=15V

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
<b>Power output section</b>						
Collector-emitter leakage current	V <sub>CE</sub> =600V	I <sub>CE</sub>	-	-	100	μA
Collector to emitter saturation voltage	I <sub>c</sub> =10A, T <sub>j</sub> =25°C	V <sub>CE(SAT)</sub>		1.9	2.7	V
	I <sub>c</sub> =5A, T <sub>j</sub> =100°C			1.6	-	V
Diode forward voltage	I <sub>F</sub> =10A, T <sub>j</sub> =25°C	V <sub>F</sub>		1.5	2.2	V
	I <sub>F</sub> =5A, T <sub>j</sub> =100°C			1.2	-	V
Junction to case thermal resistance	IGBT	θ <sub>j-c</sub> (T)	-	-	4	°C/W
	Freewheeling Diode	θ <sub>j-c</sub> (T)	-	-	5.5	°C/W
Switching time	I <sub>c</sub> =10A, V <sub>CC</sub> =300V, T <sub>j</sub> =25°C	t <sub>ON</sub>	-	0.6	1.3	μs
		t <sub>OFF</sub>	-	1.0	1.6	
Turn-on switching loss	I <sub>c</sub> =10A, V <sub>CC</sub> =300V, T <sub>j</sub> =25°C	E <sub>ON</sub>	-	300	-	μJ
Turn-off switching loss		E <sub>OFF</sub>	-	90	-	μJ
Total switching loss		E <sub>TOT</sub>	-	390	-	μJ
Turn-on switching loss	I <sub>c</sub> =10A, V <sub>CC</sub> =300V, T <sub>j</sub> =25°C	E <sub>ON</sub>	-	360	-	μJ
Turn-off switching loss		E <sub>OFF</sub>	-	110	-	μJ
Total switching loss		E <sub>TOT</sub>	-	470	-	μJ
Diode reverse recovery energy	I <sub>c</sub> =10A, V <sub>CC</sub> =300V, T <sub>j</sub> =25°C (di/dt set by internal driver)	E <sub>REC</sub>	-	60	-	μJ
Diode reverse recovery time		t <sub>rr</sub>	-	160	-	ns
Reverse bias safe operating area	I <sub>c</sub> =20A, V <sub>CE</sub> =450V	RBSOA	Full Square	-		
Short circuit safe operating area	V <sub>CE</sub> =400V	SCSOA	4	-	-	μs
Allowable offset voltage slew rate	U to NU, V to NV, W to NW	dv/dt	-50	-	50	V/ns
<b>Driver Section</b>						
Gate driver consumption current	V <sub>BS</sub> =15V (Note 4), per driver	I <sub>D</sub>	-	0.07	0.4	mA
	V <sub>DD</sub> =15V, total	I <sub>D</sub>	-	0.95	3	mA
High level Input voltage	HINU, HINV, HINW, LINU, LINV, LINW to GND	V <sub>in H</sub>	2.5	-	-	V
Low level Input voltage		V <sub>in L</sub>	-	-	0.8	V
Logic 1 input current	V <sub>IN</sub> =+3.3V	I <sub>IN+</sub>	-	660	900	μA
Logic 0 input current	V <sub>IN</sub> =0V	I <sub>IN-</sub>	-	-	3	μA
Bootstrap ON Resistance	I <sub>B</sub> =1mA	R <sub>B</sub>	-	110	-	Ω
FAULT terminal sink current	FAULT : ON / V <sub>FAULT</sub> =0.1V	I <sub>oSD</sub>	-	2	-	mA
FAULT clearance delay time	R <sub>CLR</sub> =2MΩ, C <sub>CLR</sub> =1nF	FL <sub>TCLR</sub>	1.1	1.65	2.2	ms
ENABLE ON/OFF voltage	V <sub>EN</sub> ON-state voltage	V <sub>EN(ON)</sub>	2.5	-	-	V
	V <sub>EN</sub> OFF-state voltage	V <sub>EN(OFF)</sub>	-	-	0.8	V
ITRIP threshold voltage	ITRIP to GND	V <sub>ITRIP</sub>	0.44	0.49	0.54	V
ITRIP to shutdown propagation delay		t <sub>ITRIP</sub>	-	1.1	-	μs
ITRIP blanking time		t <sub>ITRIPBL</sub>	250	350	-	ns
V <sub>DD</sub> and V <sub>BS</sub> supply undervoltage positive going input threshold		V <sub>DDUV+</sub> V <sub>B SUV+</sub>	10.2	11.1	11.8	V
V <sub>DD</sub> and V <sub>BS</sub> supply undervoltage negative going input threshold		V <sub>DDUV-</sub> V <sub>B SUV-</sub>	10.0	10.9	11.6	V
V <sub>DD</sub> and V <sub>BS</sub> supply undervoltage I <sub>lockout</sub> hysteresis		V <sub>DDUVH</sub> V <sub>B SUVH</sub>	-	0.2	-	V

7. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# STK5Q4U362J-E

## TYPICAL CHARACTERISTICS

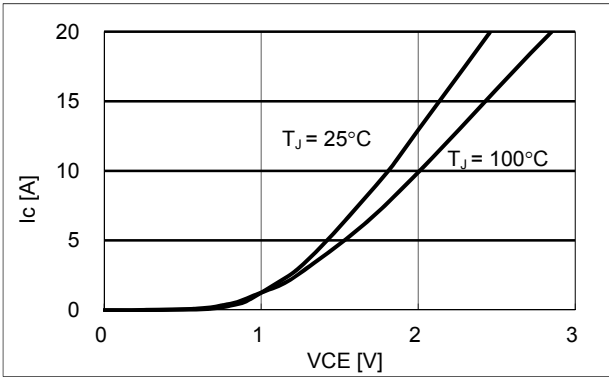


Figure 5 VCE versus ID for different temperatures (VDD=15V)

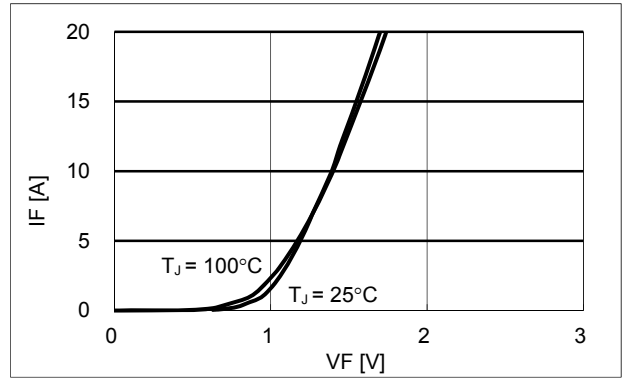


Figure 4 VF versus ID for different temperatures

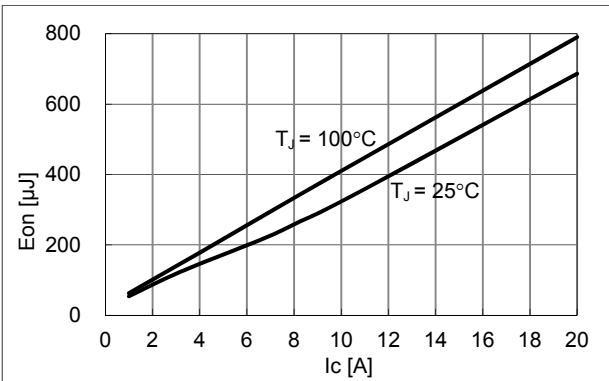


Figure 7 EON versus ID for different temperatures

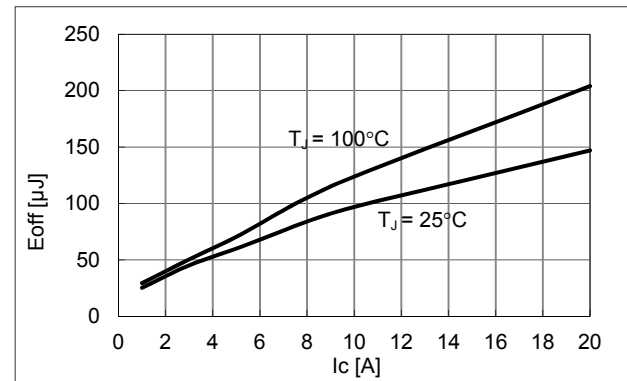


Figure 6 EOFF versus ID for different temperatures

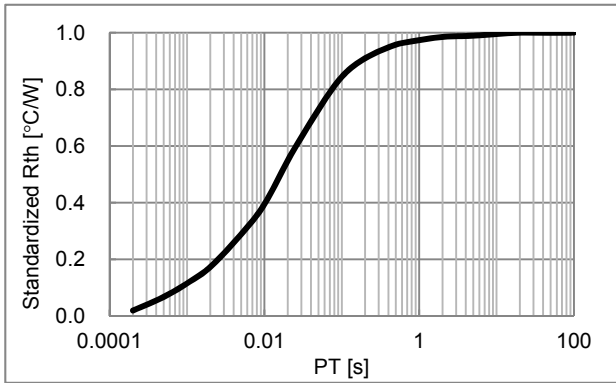


Figure 8 Thermal impedance plot (IGBT)

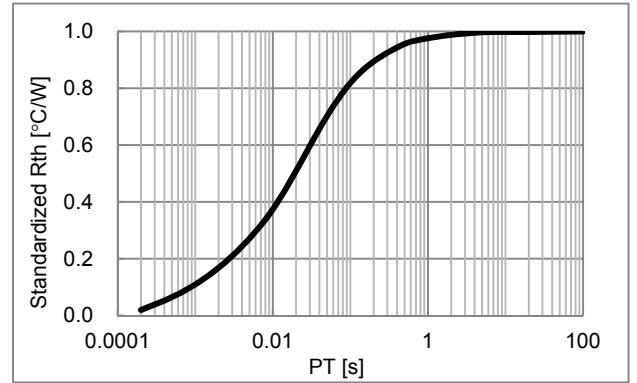


Figure 9 Thermal impedance plot (FRD)

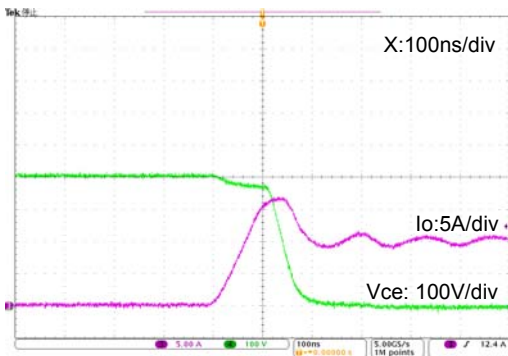


Figure 10 Turn-on waveform Tj=100°C, VCC=400V

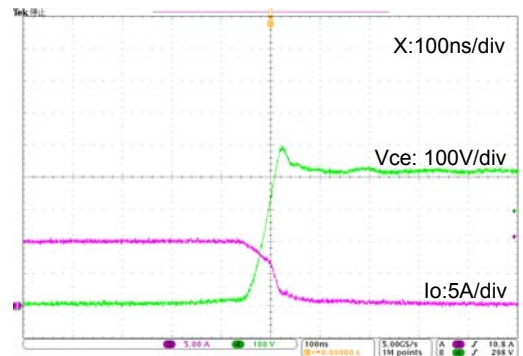


Figure 11 Turn-off waveform Tj=100°C, VCC=400V

# STK5Q4U362J-E

## APPLICATIONS INFORMATION

### Input / Output Timing Chart

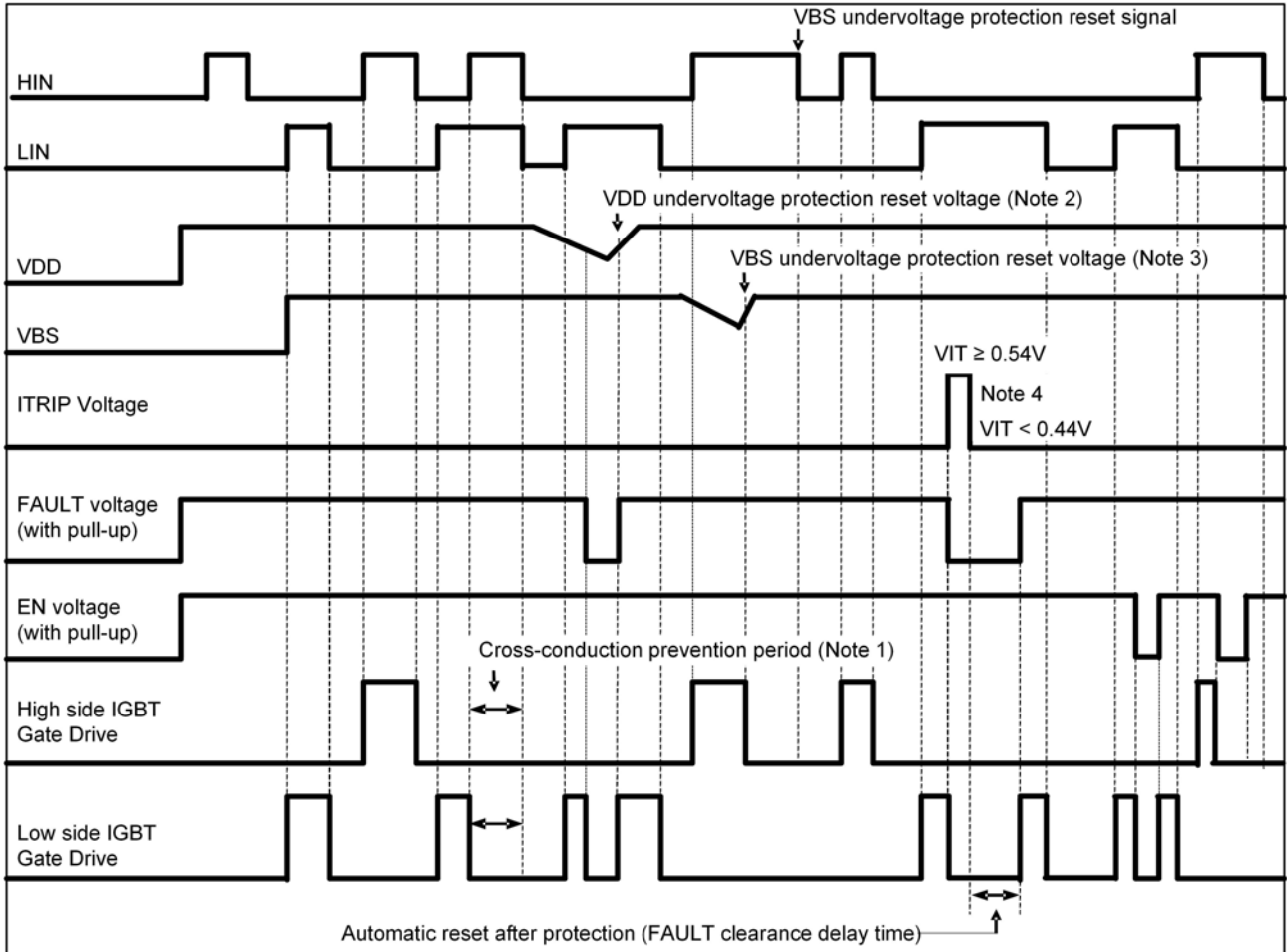


Figure 12. Input/Output Timing Chart

#### Notes

1. This section of the timing diagram shows the effect of cross-conduction prevention.
2. This section of the timing diagram shows that when the voltage on VDD decreases sufficiently all gate output signals will go low, switching off all six IGBTs. When the voltage on VDD rises sufficiently, normal operation will resume.
3. This section shows that when the bootstrap voltage VBS drops, the corresponding high side output (U or V or W) is switched off. When VBS rises sufficiently, normal operation will resume.
4. This section shows that when the voltage on ITRIP exceeds the threshold, all IGBT's are turned off. Normal operation resumes later after the over-current condition is removed.
5. After VDD has risen above the threshold to enable normal operation, the driver waits to receive an input signal on the LIN input before enabling the driver for the HIN signal.

### Input / Output Logic Table

INPUT				OUTPUT			
HIN	LIN	Itrip	Enable	High side IGBT	Low side IGBT	U,V,W	FAULT
H	L	L	H	ON (Note 5)	OFF	VP	OFF
L	H	L	H	OFF	ON	NU,NV,NW	OFF
L	L	L	H	OFF	OFF	High Impedance	OFF
H	H	L	H	OFF	OFF	High Impedance	OFF
X	X	H	H	OFF	OFF	High Impedance	ON
X	X	X	L	OFF	OFF	High Impedance	OFF



# STK5Q4U362J-E

## Thermistor characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Resistance	R <sub>25</sub>	T <sub>c</sub> =25°C	99	100	101	kΩ
	R <sub>100</sub>	T <sub>c</sub> =100°C	5.18	5.38	5.60	kΩ
B-Constant (25 to 50°C)	B		4208	4250	4293	K
Temperature Range			-40		+125	°C

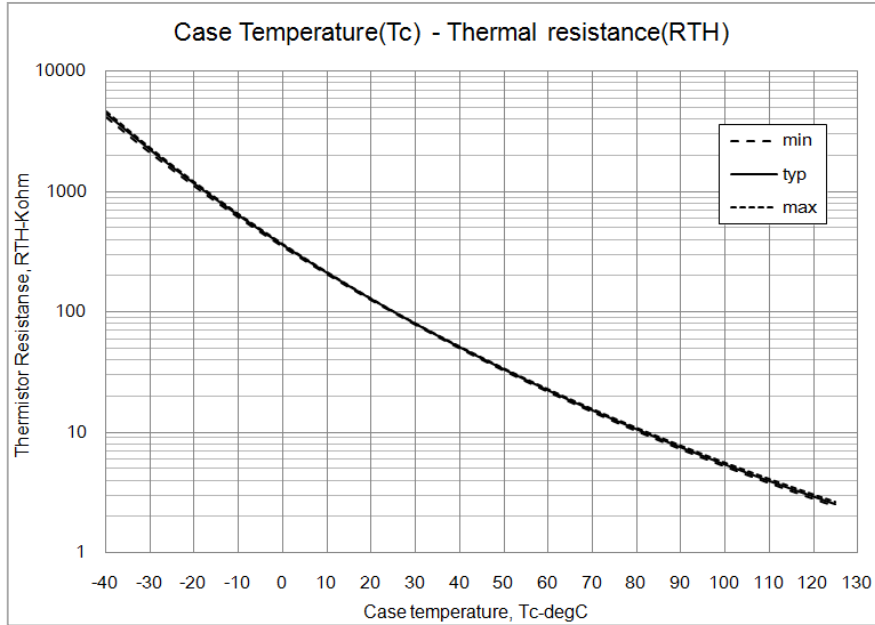


Figure 9 Thermistor Resistance versus Case Temperature

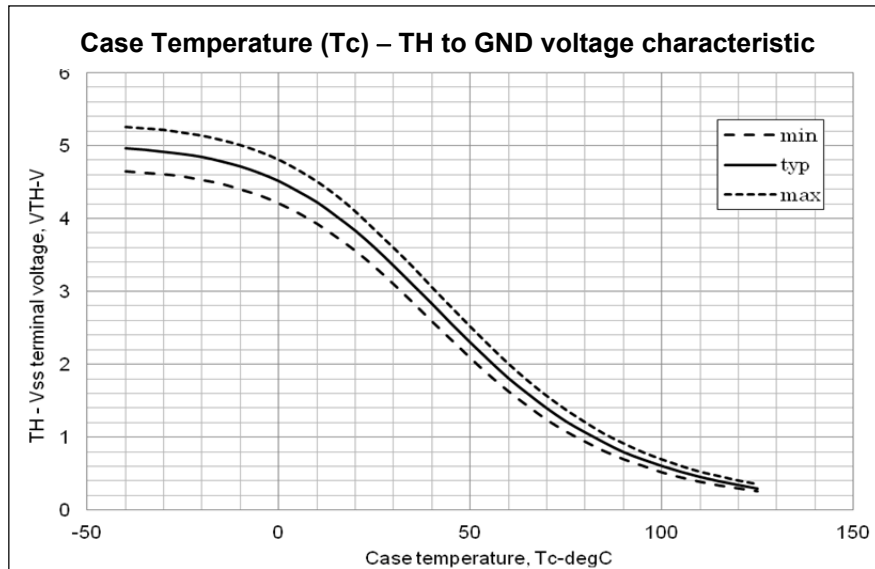


Figure 12 Thermistor Voltage versus Case Temperature  
Conditions: R<sub>TH</sub>=39kΩ, pull-up voltage 5.0V (see

Figure 2)

**Fault output**

The FAULT output is an open drain output requiring a pull-up resistor. If the pull-up voltage is 5V, use a pull-up resistor with a value of 6.8kΩ or higher. If the pull-up voltage is 15V, use a pull-up resistor with a value of 20kΩ or higher. The FAULT output is triggered if there is a VDD undervoltage or an overcurrent condition.

**Undervoltage lockout protection**

If VDD goes below the VDD supply undervoltage lockout falling threshold, the FAULT output is switched on. The FAULT output stays on until VDD rises above the VDD supply undervoltage lockout rising threshold. After VDD has risen above the threshold to enable normal operation, the driver waits to receive an input signal on the LIN input before enabling the driver for the HIN signal.

**Overcurrent protection**

An over-current condition is detected if the voltage on the ITRIP pin is larger than the reference voltage. There is a blanking time of typically 350ns to improve noise immunity. After a shutdown propagation delay of typically 1.1 us, the FAULT output is switched on. The FAULT output is held on for a time determined by the resistor and capacitor connected to the RCIN pin. If RCLR=2MΩ and CCLR=1nF, the FAULT output is switched on for 1.65ms (typical).

The over-current protection threshold should be set to be equal or lower to 2 times the module rated current (IO).

An additional fuse is recommended to protect against system level or abnormal over-current fault conditions.

**Capacitors on High Voltage and VDD supplies**

Both the high voltage and VDD supplies require an electrolytic capacitor and an additional high frequency capacitor.

**Enable pin**

The ENABLE terminal pin is used to enable or shut down the built-in driver. If the voltage on the ENABLE pin rises above the ENABLE ON-state voltage the output drivers are enabled. If the voltage on the ENABLE pin falls below the ENABLE OFF-state voltage, the drivers are disabled.

**Minimum input pulse width**

When input pulse width is less than 1μs, an output may not react to the pulse. (Both ON signal and OFF signal)

**Calculation of bootstrap capacitor value**

The bootstrap capacitor value CB is calculated using the following approach. The following parameters influence the choice of bootstrap capacitor:

- VBS: Bootstrap power supply. 15V is recommended.
- QG: Total gate charge of IGBT at VBS=15V. 45nC
- UVLO: Falling threshold for UVLO. Specified as 12V.
- ID<sub>MAX</sub>: High side drive consumption current.. Specified as 0.4mA
- t<sub>ONMAX</sub>: Maximum ON pulse width of high side IGBT.

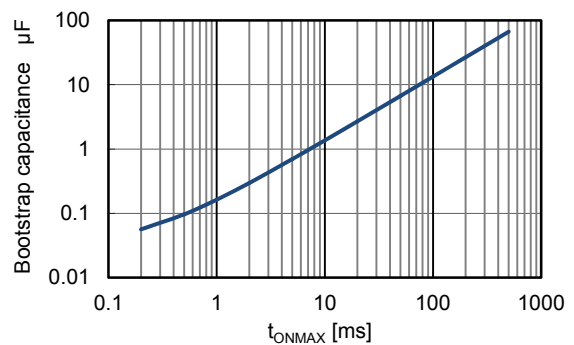
Capacitance calculation formula:

$$CB = (QG + I_{D_{MAX}} * t_{ONMAX}) / (VBS - UVLO)$$

CB is recommended to be approximately 3 times the value calculated above. The recommended value of CB is in the range of 1 to 47μF, however, the value needs to be verified prior to production. When not using the bootstrap circuit, each high side driver power supply requires an external independent power supply.

The internal bootstrap circuit uses a MOSFET. The turn on time of this MOSFET is synchronized with the turn on of the low side IGBT. The bootstrap capacitor is charged by turning on the low side IGBT.

If the low side IGBT is held on for a long period of time (more than one second for example), the bootstrap voltage on the high side MOSFET will slowly discharge.



**Figure 13: Bootstrap capacitance versus t<sub>ONMAX</sub>**

# STK5Q4U362J-E

## Mounting Instructions

Item	Recommended Condition
Pitch	26.0±0.1mm (Please refer to Package Outline Diagram)
Screw	Diameter : M3 Screw head types: pan head, truss head, binding head
Washer	Plane washer dimensions (Figure 14) D = 7mm, d = 3.2mm and t = 0.5mm JIS B 1256
Heat sink	Material: Aluminum or Copper Warpage (the surface that contacts IPM) : -50 to 50 μm Screw holes must be countersunk. No contamination on the heat sink surface that contacts IPM.
Torque	Temporary tightening : 50 to 60 % of final tightening on first screw Temporary tightening : 50 to 60 % of final tightening on second screw Final tightening : 0.4 to 0.6Nm on first screw Final tightening : 0.4 to 0.6Nm on second screw
Grease	Silicone grease. Thickness : 50 to 100 μm Uniformly apply silicon grease to whole back. Thermal foils are only recommended after careful evaluation. Thickness, stiffness and compressibility parameters have a strong influence on performance.

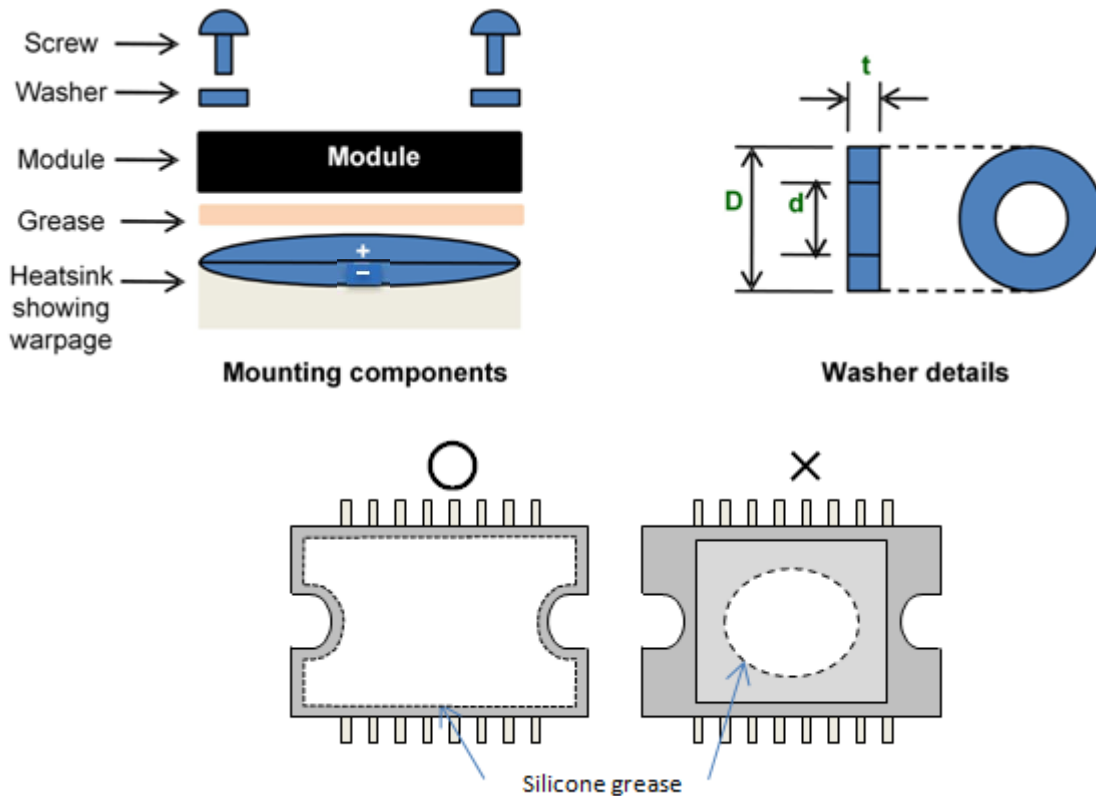


Figure 14: Module Mounting details: components; washer drawing; need for even spreading of thermal grease

# STK5Q4U362J-E

## TEST CIRCUITS

### ■ ICE

	U+	V+	W+	U-	V-	W-
M	38	38	38	32	26	20
N	32	26	20	17	18	19

U+,V+,W+ : High side phase  
 U-,V-,W- : Low side phase

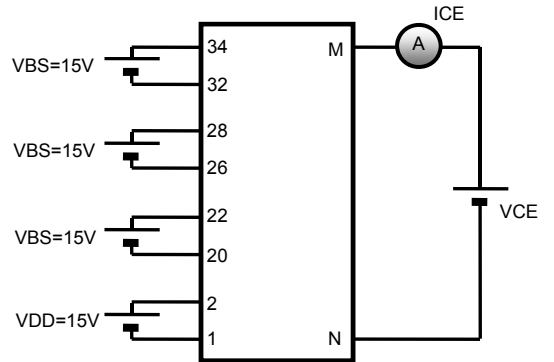


Figure 15 Test Circuit for ICE

### ■ VCE(sat) (Test by pulse)

	U+	V+	W+	U-	V-	W-
M	38	38	38	32	26	20
N	32	26	20	17	18	19
m	3	4	5	6	7	8

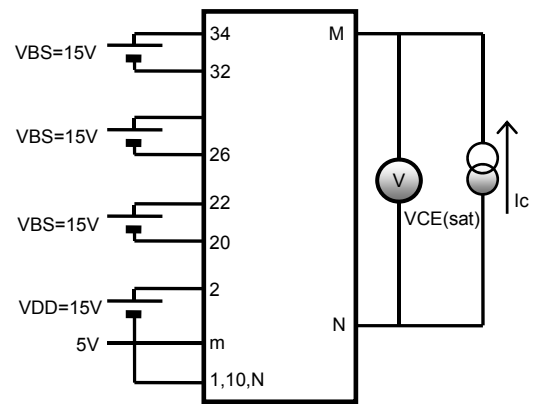


Figure 16 Test circuit for VCE(sat)

### ■ VF (Test by pulse)

	U+	V+	W+	U-	V-	W-
M	38	38	38	32	26	20
N	32	26	20	17	18	19

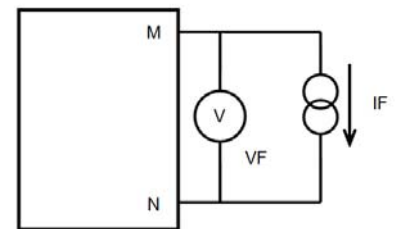


Figure 17 Test circuit for VF

# STK5Q4U362J-E

## ■ RB (Test by pulse)

	U+	V+	W+
M	2	2	2
N	34	28	22

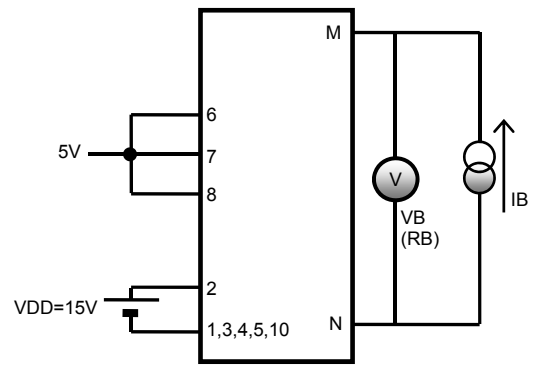


Figure 18 Test circuit for RB

## ■ ID

	VBS U+	VBS V+	VBS W+	VDD
M	34	28	22	2
N	32	26	20	1

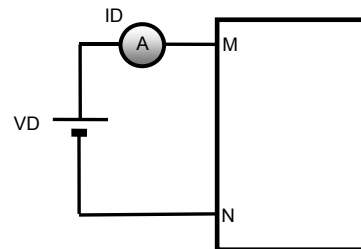


Figure 19 Test circuit for ID

## ■ Switching time (The circuit is a representative example of the low side U phase.)

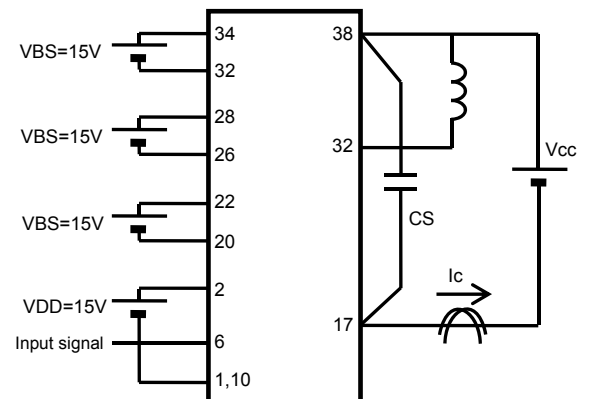
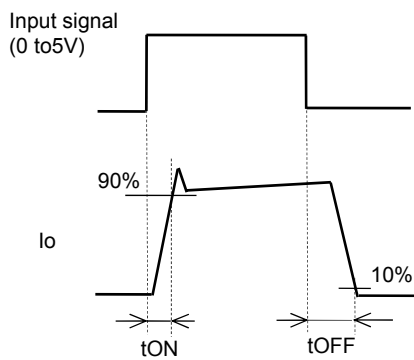
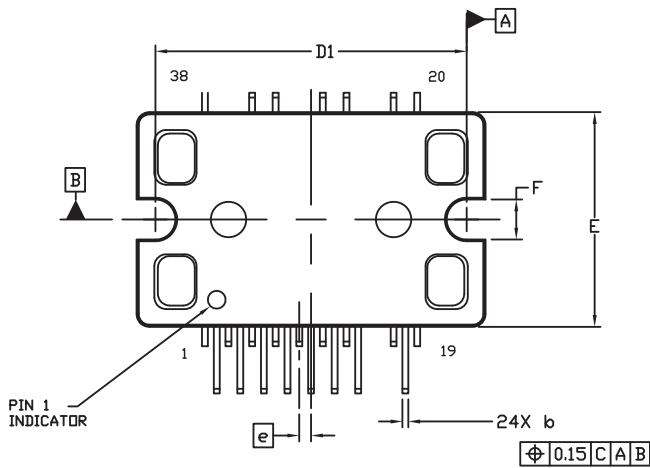


Figure 20 Switching time test circuit

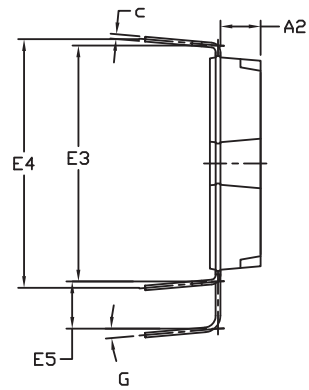
# STK5Q4U362J-E

## PACKAGE DIMENSIONS

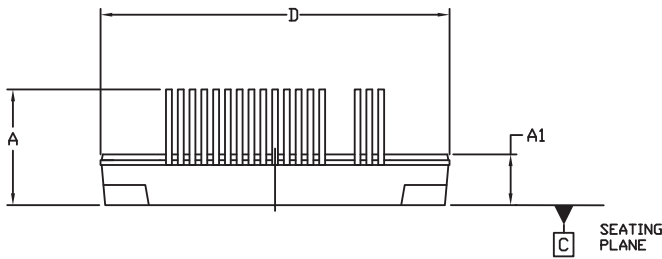
unit : mm



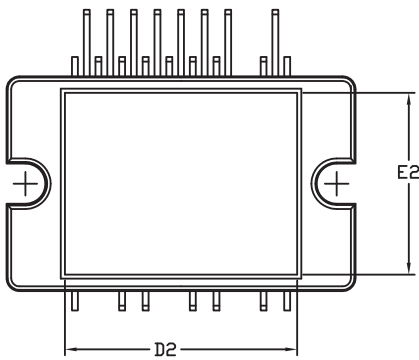
TOP VIEW



END VIEW



SIDE VIEW



BOTTOM VIEW

### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED LEAD AND IS MEASURED BETWEEN 0.10 AND 0.25 FROM THE LEAD TIP.
4. PACKAGE IS MISSING PINS: 15, 16, 21, 23, 24, 25, 27, 29, 30, 31, 33, 35, 36, AND 37.

DIM	MILLIMETERS	
	MIN.	MAX.
A	9.30	10.30
A1	3.80	4.80
A2	2.90	3.90
b	0.45	0.70
c	0.35	0.60
D	29.10	30.10
D1	26.30	26.50
D2	19.20	20.20
E	17.70	18.70
E2	14.90	15.90
E3	19.50	20.50
E4	21.10	REF
E5	3.50	4.50
e	1.00	BSC
F	2.90	3.90
G	4°	6°

ON Semiconductor and the ON logo are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[ON Semiconductor:](#)

[STK5Q4U362J-E](#)