

# NVLJD4007NZ

## Small Signal MOSFET

30 V, 245 mA, Dual, N-Channel, Gate ESD Protection, 2x2 WDFN Package

### Features

- Optimized Layout for Excellent High Speed Signal Integrity
- Low Gate Charge for Fast Switching
- Small 2 x 2 mm Footprint
- ESD Protected Gate
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	$V_{DSS}$	30	V	
Gate-to-Source Voltage	$V_{GS}$	$\pm 10$	V	
Continuous Drain Current (Note 1)	$I_D$	Steady State = $25^\circ\text{C}$	245	mA
Power Dissipation (Note 1)		Steady State = $25^\circ\text{C}$	$P_D$	755
Pulsed Drain Current	$I_{DM}$	$t_p \leq 10 \mu\text{s}$	1.2	A
Operating Junction and Storage Temperature		$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$
Continuous Source Current (Body Diode)	$I_{SD}$	245	mA	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	166	$^\circ\text{C}/\text{W}$

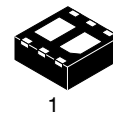
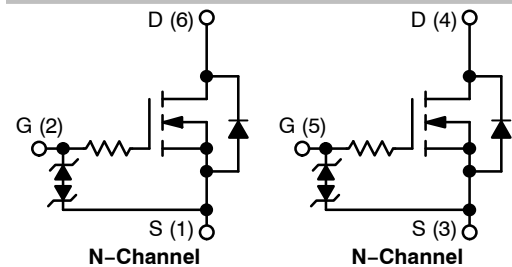
1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).



ON Semiconductor®

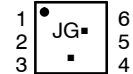
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ Typ @ $V_{GS}$	$I_D$ MAX (Note 1)
30 V	1.4 $\Omega$ @ 4.5 V	245 mA
	2.3 $\Omega$ @ 2.5 V	



### MARKING DIAGRAM

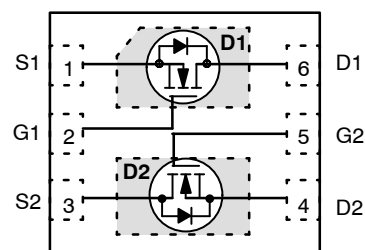
WDFN6  
CASE 506AN



JG = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### PIN CONNECTIONS



(Top View)

### ORDERING INFORMATION

Device	Package	Shipping†
NVLJD4007NZZTAG	WDFN6 (Pb-Free)	3000/Tape & Reel
NVLJD4007NZZTBG	WDFN6 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NVLJD4007NZ

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
-----------	--------	----------------	-----	-----	-----	------

### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 100 μA	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>	Reference to 25°C, I <sub>D</sub> = 100 μA		27		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 30 V			1.0	μA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 20 V, T = 85 °C			1.0	μA
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±10 V			±25	μA
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±5 V			±1.0	μA
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±5 V, T = 85 °C			±1.0	μA

### ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 100 μA	0.5	1.0	1.5	V
Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>	Reference to 25°C, I <sub>D</sub> = 100 μA		-2.5		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 125 mA		1.4	7.0	Ω
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 125 mA		2.3	7.5	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 3 V, I <sub>D</sub> = 125 mA		80		mS

### CAPACITANCES & GATE CHARGE

Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> = 5.0 V, f = 1 MHz, V <sub>GS</sub> = 0 V		12.2	20	pF
Output Capacitance	C <sub>OSS</sub>			10	15	
Reverse Transfer Capacitance	C <sub>RSS</sub>			3.3	6.0	
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 24 V, I <sub>D</sub> = 100 mA, V <sub>GS</sub> = 4.5 V		0.75		nC
Gate-to-Source Charge	Q <sub>gs</sub>			0.20		
Gate-to-Drain Charge	Q <sub>gd</sub>			0.20		
Plateau Voltage	V <sub>GP</sub>			1.57		V

### SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 24 V, I <sub>D</sub> = 125 mA, R <sub>G</sub> = 10 Ω		9		ns
Rise Time	t <sub>r</sub>			41		ns
Turn-Off Delay Time	t <sub>d(OFF)</sub>			96		
Fall Time	t <sub>f</sub>			72		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 125 mA		0.79	0.9	V
-----------------------	-----------------	--	--	------	-----	---

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

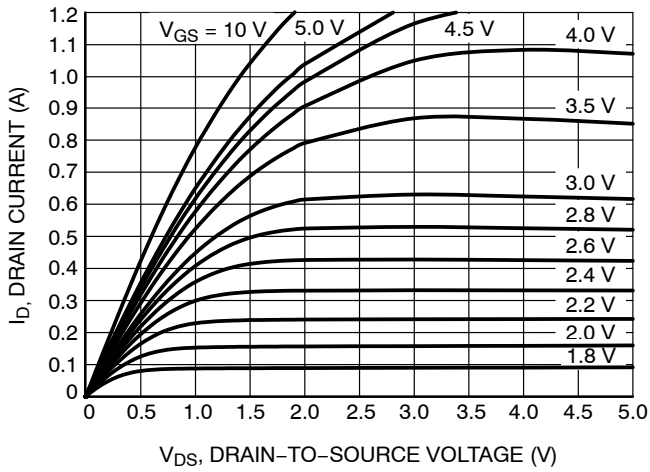


Figure 1. On-Region Characteristics

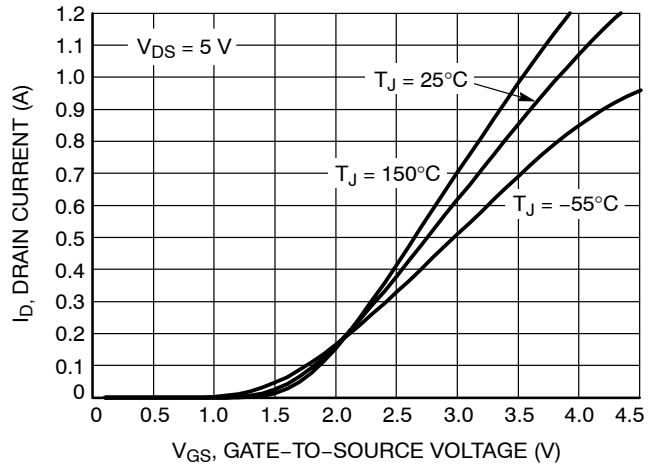


Figure 2. Transfer Characteristics

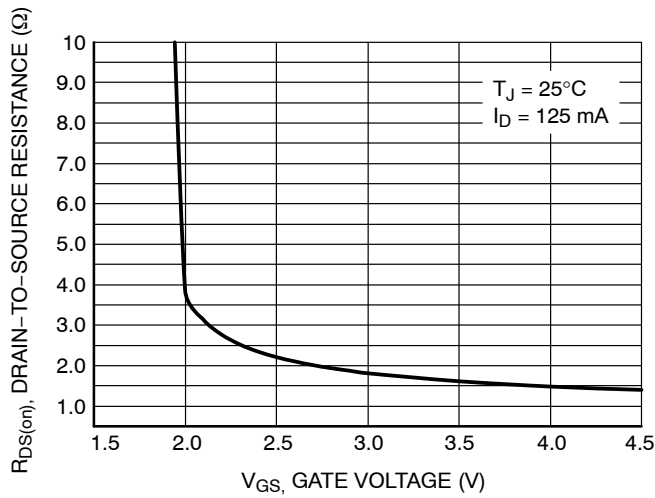


Figure 3. On-Resistance vs. Gate-to-Source Voltage

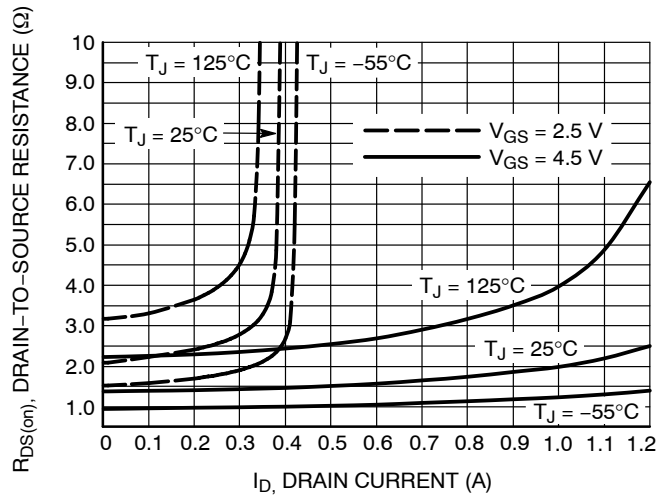


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

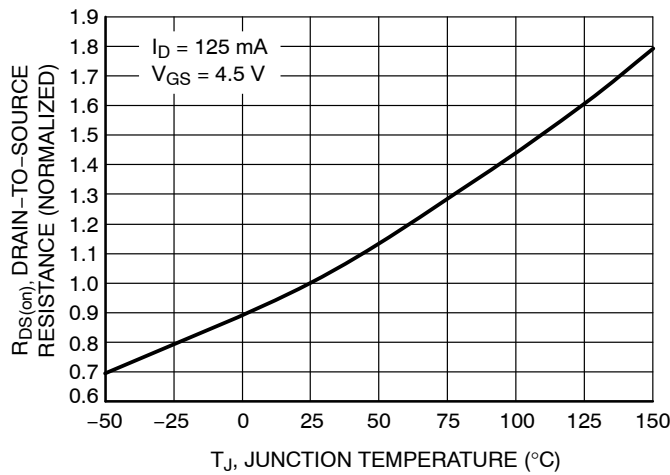


Figure 5. On-Resistance Variation with Temperature

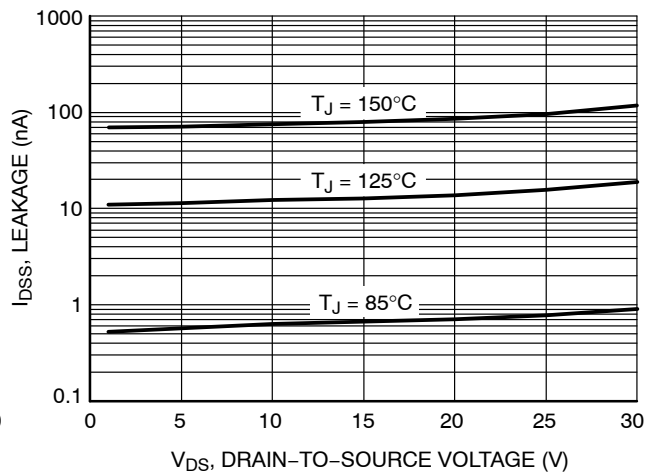


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

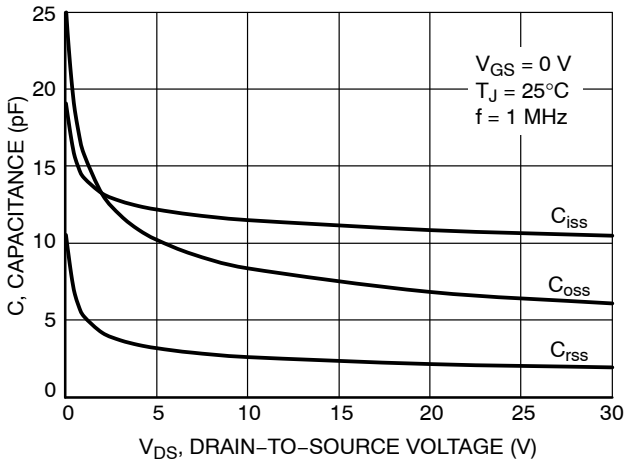


Figure 7. Capacitance Variation

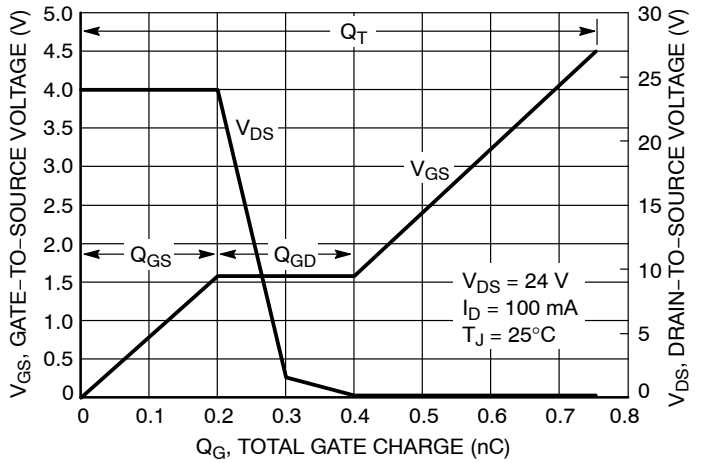


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

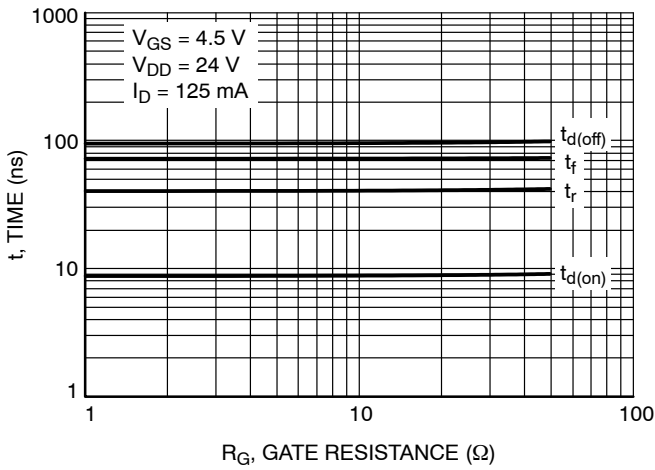


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

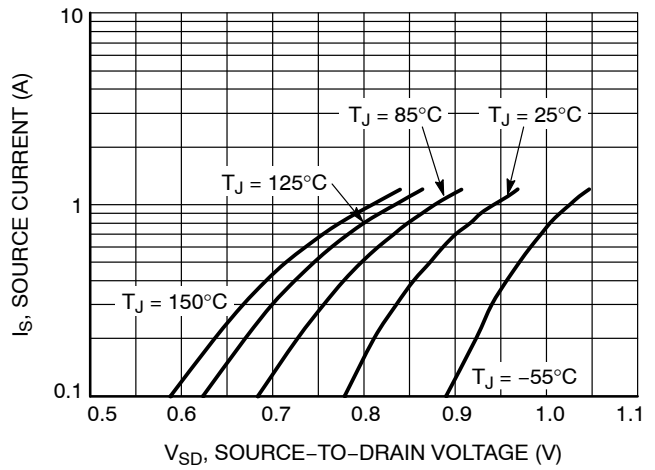


Figure 10. Diode Forward Voltage vs. Current

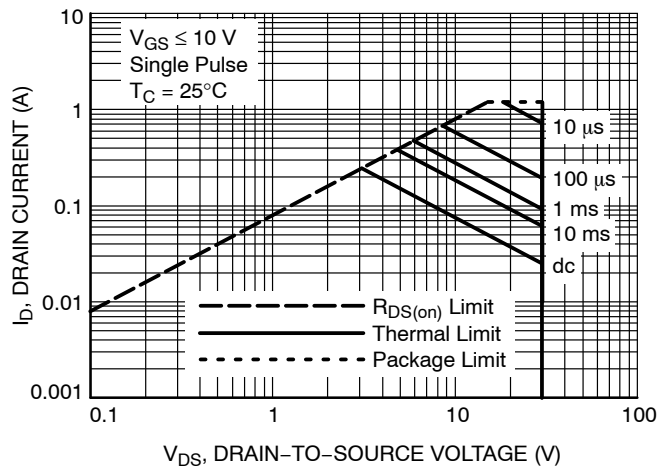


Figure 11. Maximum Rated Forward Biased Safe Operating Area

TYPICAL PERFORMANCE CURVES

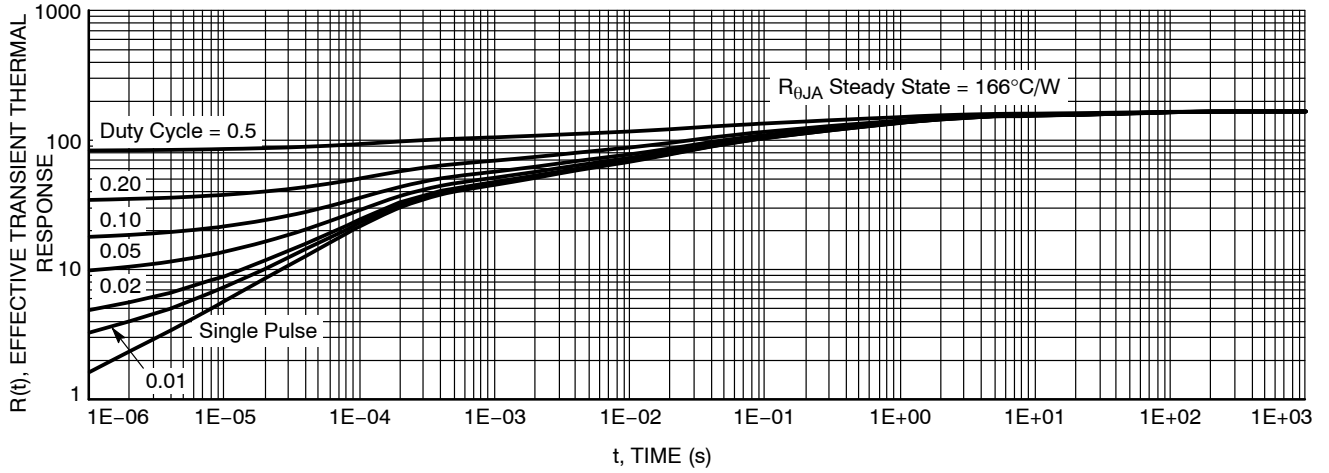
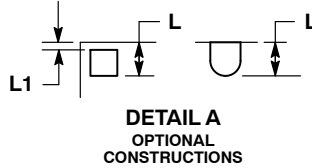
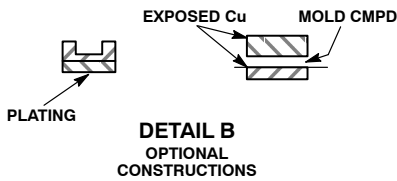
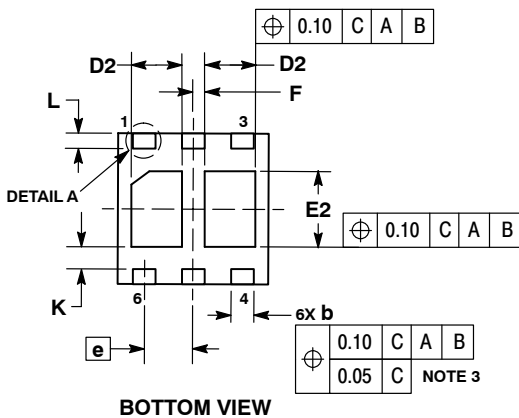
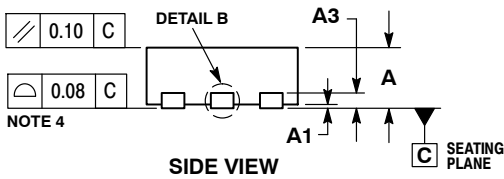
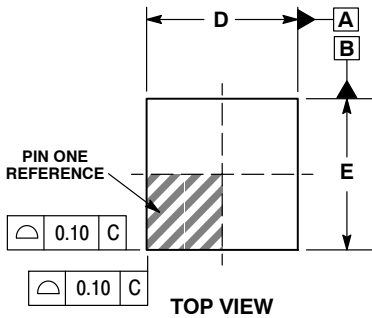


Figure 12. Thermal Impedance (Junction-to-Ambient)

# NVLJD4007NZ

## PACKAGE DIMENSIONS

WDFN6 2x2, 0.65P  
CASE 506AN  
ISSUE F



**NOTES:**

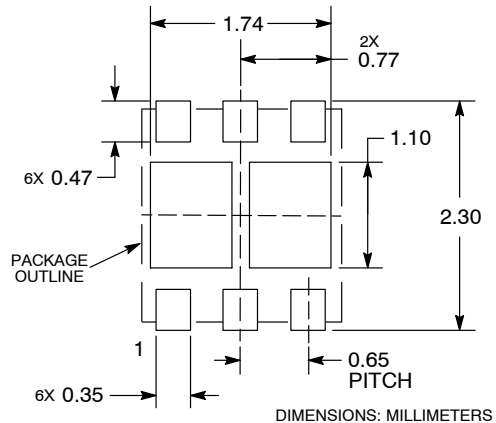
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	2.00 BSC	
D2	0.57	0.77
E	2.00 BSC	
E2	0.90	1.10
e	0.65 BSC	
F	0.15 BSC	
K	0.25 REF	
L	0.20	0.30
L1	---	0.10

**STYLE 3:**

1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. DRAIN 2
5. GATE 2
6. DRAIN 1

### SOLDERMASK DEFINED MOUNTING FOOTPRINT



**ON Semiconductor** and **ON** are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)

**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[ON Semiconductor:](#)

[NVLJD4007NZTAG](#)