

NSTB60BDW1

PNP General Purpose and NPN Bias Resistor Transistor Combination

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Available in 8 mm, 7 inch/3000 Unit Tape and Reel
- ESD Rating – Human Body Model: Class 1B
– Machine Model: Class B
- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted, common for Q_1 and Q_2)

Rating	Symbol	Q_1	Q_2	Unit
Collector-Emitter Voltage	V_{CEO}	-50	50	Vdc
Collector-Base Voltage	V_{CBO}	-50	50	Vdc
Emitter-Base Voltage	V_{EBO}	-6.0	5.0	Vdc
Collector Current – Continuous	I_C	-150	150	mAdc

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

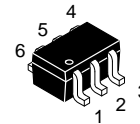
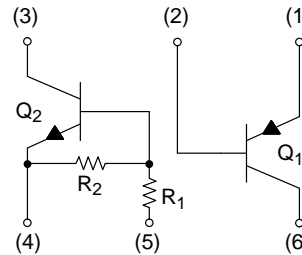
Characteristic (One Junction Heated)	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	187 (Note 1) 256 (Note 2) 1.5 (Note 1) 2.0 (Note 2)	mW mW/ $^\circ\text{C}$
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	670 (Note 1) 490 (Note 2)	$^\circ\text{C}/\text{W}$
Characteristic (Both Junctions Heated)	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	250 (Note 1) 385 (Note 2) 2.0 (Note 1) 3.0 (Note 2)	mW mW/ $^\circ\text{C}$
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	493 (Note 1) 325 (Note 2)	$^\circ\text{C}/\text{W}$
Thermal Resistance – Junction-to-Lead	$R_{\theta JL}$	188 (Note 1) 208 (Note 2)	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

1. FR-4 @ Minimum Pad
2. FR-4 @ 1.0 x 1.0 inch Pad



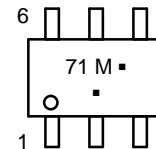
ON Semiconductor®

www.onsemi.com



SOT-363
CASE 419B
STYLE 1

MARKING DIAGRAM



71 = Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)
*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
NSTB60BDW1T1G	SOT-363 (Pb-Free)	3000 / Tape & Reel
NSVTB60BDW1T1G	SOT-363 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NSTB60BDW1

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Q₁					
Collector-Base Breakdown Voltage ($I_C = -50 \mu\text{Adc}$, $I_E = 0$)	$V_{(BR)CBO}$	-50	-	-	Vdc
Collector-Emitter Breakdown Voltage ($I_C = -1.0 \text{ mAdc}$, $I_B = 0$)	$V_{(BR)CEO}$	-50	-	-	Vdc
Emitter-Base Breakdown Voltage ($I_E = -50 \mu\text{Adc}$, $I_C = 0$)	$V_{(BR)EBO}$	-6.0	-	-	Vdc
Collector-Base Cutoff Current ($V_{CB} = -50 \text{ Vdc}$, $I_E = 0$)	I_{CBO}	-	-	-0.1	μA
Emitter-Base Cutoff Current ($V_{EB} = -6.0 \text{ Vdc}$, $I_B = 0$)	I_{EBO}	-	-	-0.1	μA
Collector-Emitter Saturation Voltage ($I_C = -50 \text{ mAdc}$, $I_B = -5.0 \text{ mAdc}$) (Note 3)	$V_{CE(sat)}$	-	-	-0.5	Vdc
DC Current Gain ($V_{CE} = -10 \text{ V}$, $I_C = -5.0 \text{ mA}$) (Note 3)	h_{FE}	120	-	560	-
Transition Frequency ($V_{CE} = -12 \text{ Vdc}$, $I_C = -2.0 \text{ mAdc}$, $f = 100 \text{ MHz}$)	f_T	-	140	-	MHz
Output Capacitance ($V_{CB} = -12 \text{ Vdc}$, $I_E = 0 \text{ Adc}$, $f = 1.0 \text{ MHz}$)	C_{OB}	-	3.5	-	pF

Q₂

Collector-Base Breakdown Voltage ($I_C = 50 \mu\text{A}$, $I_E = 0$)	$V_{(BR)CBO}$	50	-	-	Vdc
Collector-Emitter Breakdown Voltage ($I_C = 1.0 \text{ mA}$, $I_B = 0$) (Note 3)	$V_{(BR)CEO}$	50	-	-	Vdc
Collector-Base Cutoff Current ($V_{CB} = 50 \text{ V}$, $I_E = 0$)	I_{CBO}	-	-	100	nAdc
Collector-Emitter Cutoff Current ($V_{CE} = 50 \text{ V}$, $I_B = 0$)	I_{CEO}	-	-	500	nAdc
Emitter-Base Cutoff Current ($V_{EB} = 6.0 \text{ V}$, $I_C = 0$)	I_{EBO}	-	-	0.13	mAdc
Collector-Emitter Saturation Voltage ($I_C = 10 \text{ mA}$, $I_B = 5.0 \text{ mA}$) (Note 3)	$V_{CE(sat)}$	-	-	0.25	Vdc
DC Current Gain ($V_{CE} = 10 \text{ V}$, $I_C = 5.0 \text{ mA}$) (Note 3)	h_{FE}	80	-	-	
Output Voltage (on) ($V_{CC} = 5.0 \text{ V}$, $V_B = 4.0 \text{ V}$, $R_L = 1.0 \text{ k}\Omega$) (Note 3)	V_{OL}	-	-	0.2	Vdc
Output Voltage (off) ($V_{CC} = 5.0 \text{ V}$, $V_B = 0.25 \text{ V}$, $R_L = 1.0 \text{ k}\Omega$) (Note 3)	V_{OH}	4.9	-	-	Vdc
Input Resistor (Note 3)	R1	15.4	22	28.6	$\text{k}\Omega$
Resistor Ratio (Note 3)	R2/R1	1.70	2.13	2.55	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

TYPICAL ELECTRICAL CHARACTERISTICS – PNP Transistor

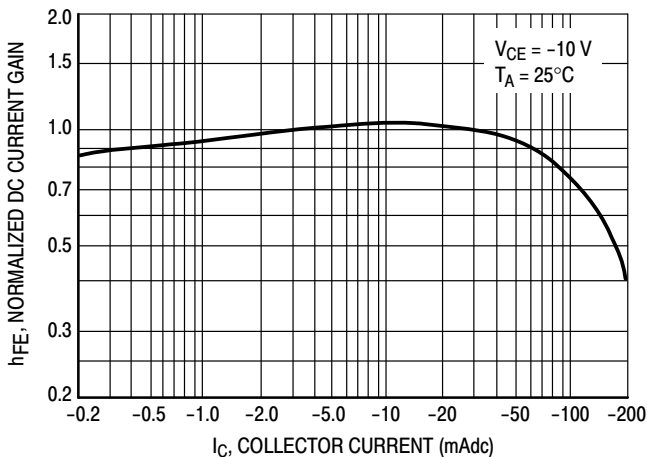


Figure 1. Normalized DC Current Gain

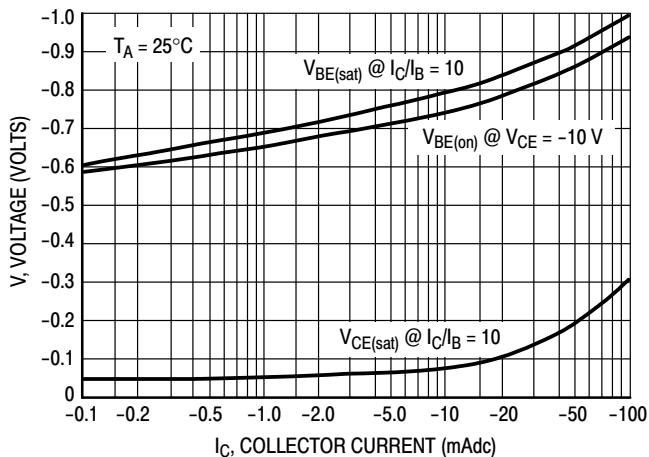


Figure 2. "Saturation" and "On" Voltages

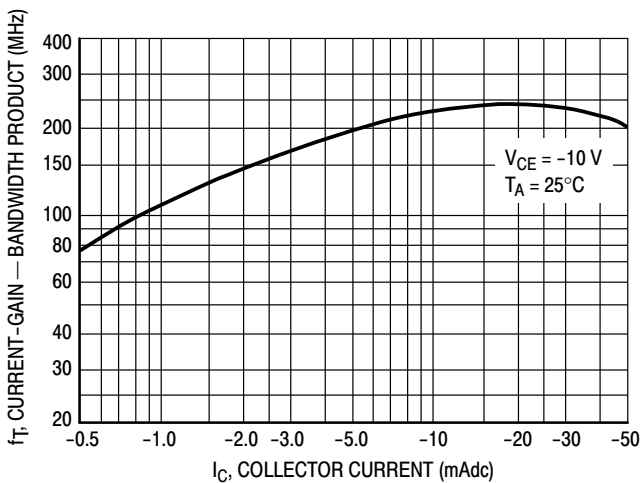


Figure 3. Current-Gain – Bandwidth Product

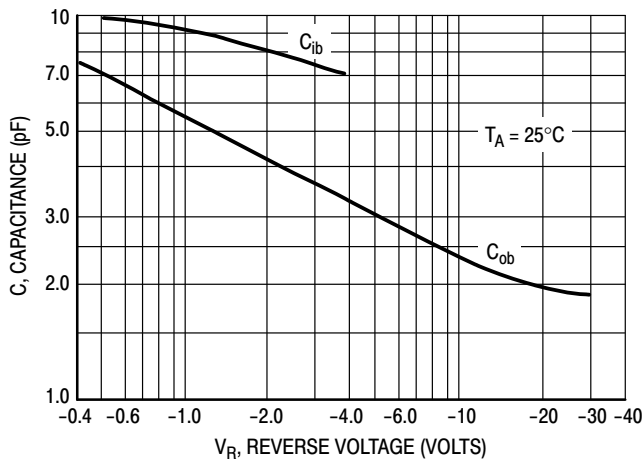


Figure 4. Capacitances

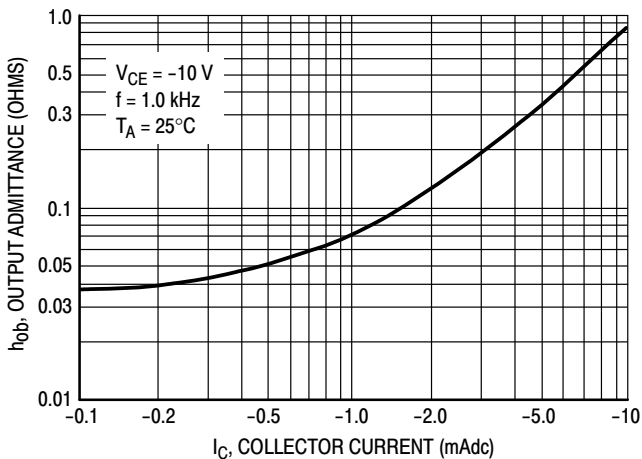


Figure 5. Output Admittance

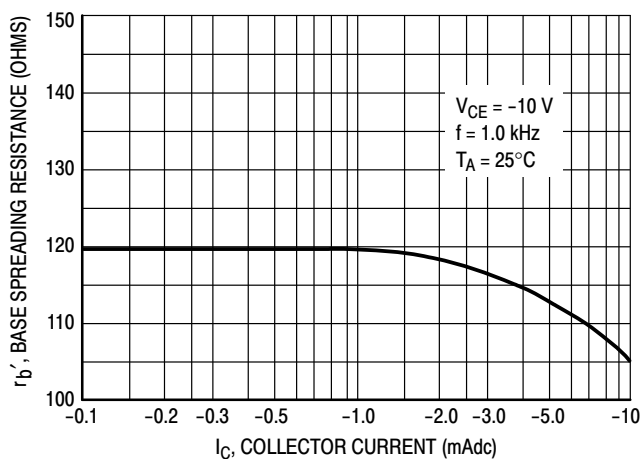


Figure 6. Base Spreading Resistance

NSTB60BDW1

TYPICAL ELECTRICAL CHARACTERISTICS – NPN Transistor

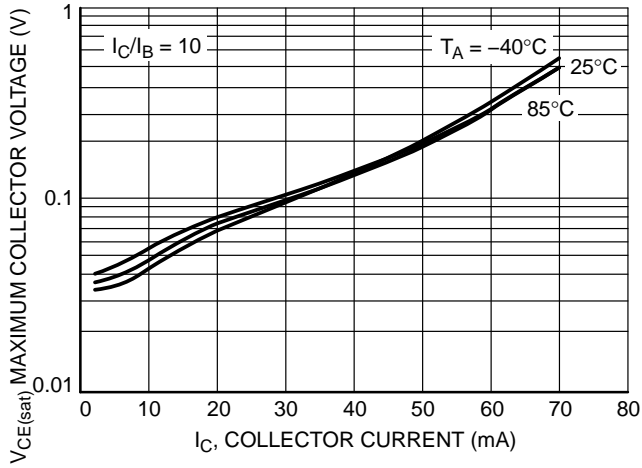


Figure 7. Maximum Collector Voltage versus Collector Current

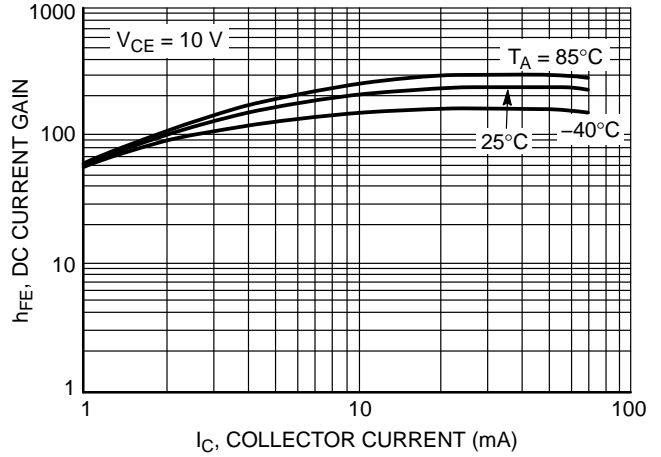


Figure 8. DC Current Gain

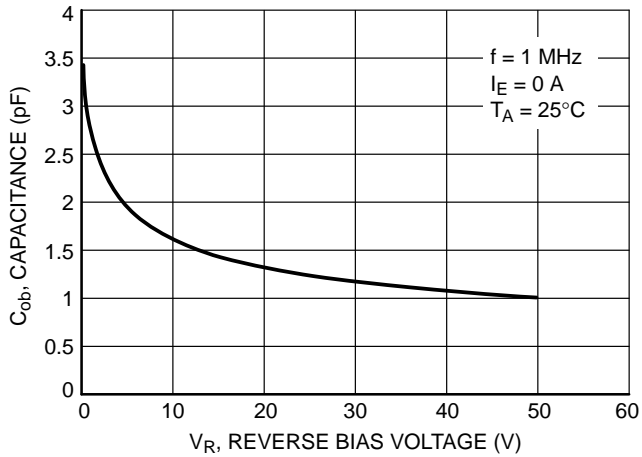


Figure 9. Output Capacitance

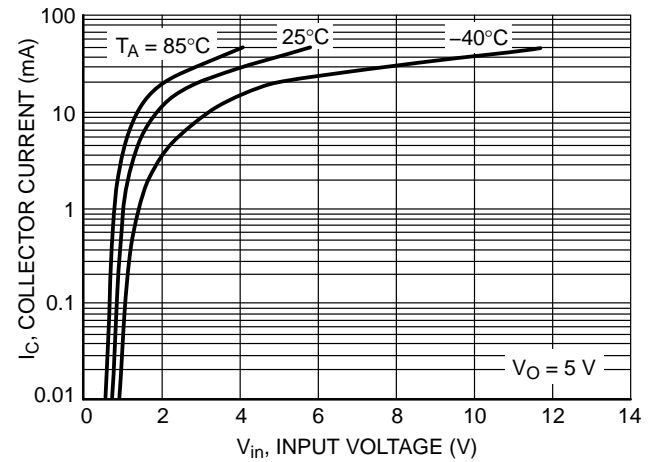


Figure 10. Output Current versus Input Voltage

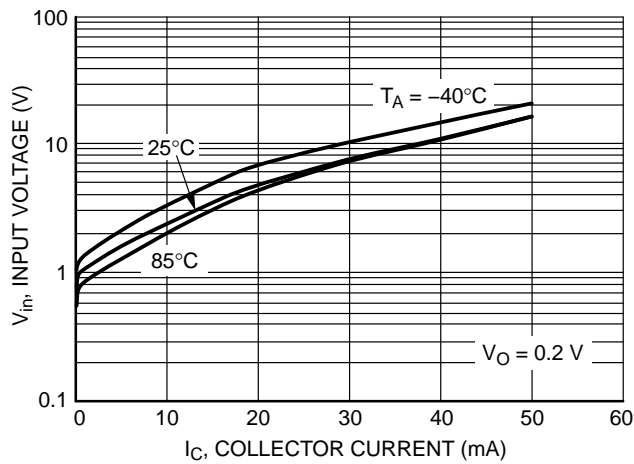
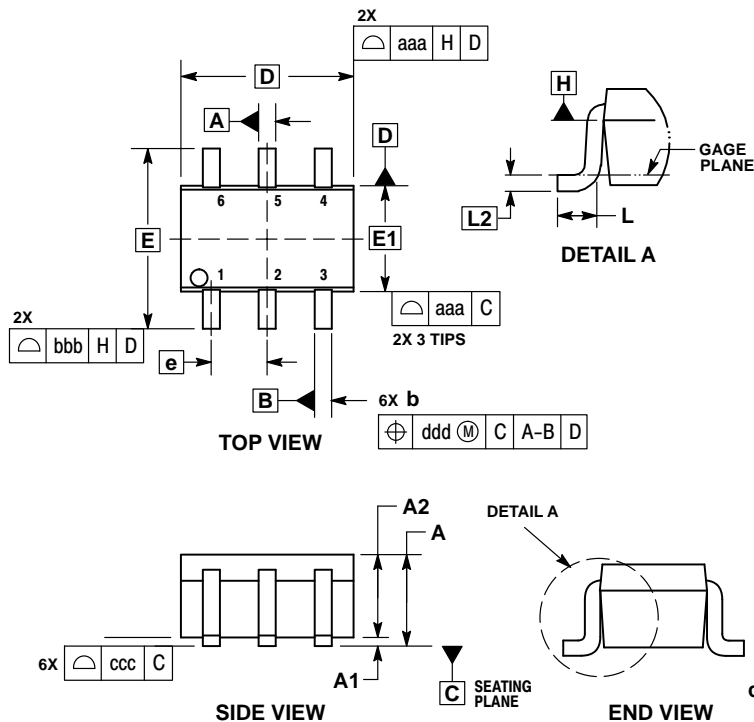


Figure 11. Input Voltage versus Output Current

NSTB60BDW1

PACKAGE DIMENSIONS

SOT-363/SC-88/SC70-6
CASE 419B-02
ISSUE Y

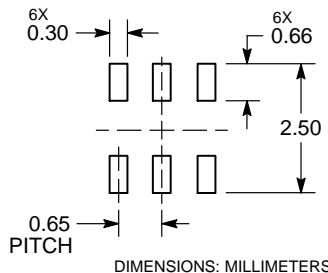


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.043
A1	0.00	---	0.10	0.000	---	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

RECOMMENDED SOLDERING FOOTPRINT*



STYLE 1:

1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and the are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marketing.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local Sales Representative

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[ON Semiconductor:](#)

[NSTB60BDW1T1G](#)