NSS12100XV6T1G

12 V, 1 A, Low $V_{CE(sat)}$ PNP Transistor

ON Semiconductor's e²PowerEdge family of low $V_{CE(sat)}$ transistors are miniature surface mount devices featuring ultra low saturation voltage ($V_{CE(sat)}$) and high current gain capability. These are designed for use in low voltage, high speed switching applications where affordable efficient energy control is important.

Typical application are DC−DC converters and power management in portable and battery powered products such as cellular and cordless phones, PDAs, computers, printers, digital cameras and MP3 players. Other applications are low voltage motor controls in mass storage products such as disc drives and tape drives. In the automotive industry they can be used in air bag deployment and in the instrument cluster. The high current gain allows e²PowerEdge devices to be driven directly from PMU's control outputs, and the Linear Gain (Beta) makes them ideal components in analog amplifiers.

Features

- High Current Capability (1 A)
- High Power Handling (Up to 650 mW)
- Low $V_{CE(s)}$ (150 mV Typical @ 500 mA)
- Small Size
- This is a Pb−Free Device

Benefits

- High Specific Current and Power Capability Reduces Required PCB Area
- Reduced Parasitic Losses Increases Battery Life

MAXIMUM RATINGS (T_A = 25°C)

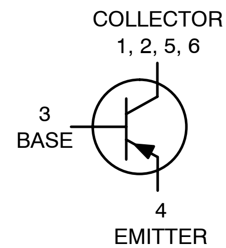
Rating	Symbol	Max	Unit
Collector-Emitter Voltage	V_{CEO}	−12	Vdc
Collector-Base Voltage	V_{CBO}	−12	Vdc
Emitter-Base Voltage	V_{EBO}	−5.0	Vdc
Collector Current − Continuous − Peak	I_C I_{CM}	−1.0 −2.0	Adc
Electrostatic Discharge	ESD	HBM Class 3 MM Class C	

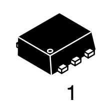
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ON Semiconductor®

http://onsemi.com

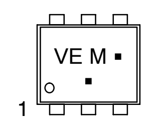
12 VOLTS, 1.0 AMPS
PNP LOW $V_{CE(sat)}$ TRANSISTOR
EQUIVALENT $R_{DS(on)}$ 300 mΩ





SOT−563
CASE 463A
STYLE 4

DEVICE MARKING



VE = Specific Device Code
M = Month Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NSS12100XV6T1G	SOT−563 (Pb−Free)	4000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

November, 2006 − Rev. 0

Publication Order Number:
NSS12100XV6/D

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation $T_A = 25°C$ Derate above 25°C	P_D (Note 1)	500 4.0	mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$ (Note 1)	250	°C/W
Total Device Dissipation $T_A = 25°C$ Derate above 25°C	P_D (Note 2)	650 5.2	mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$ (Note 2)	192	°C/W
Thermal Resistance, Junction−to−Lead 6	$R_{\theta JL}$	105	°C/W
Total Device Dissipation (Single Pulse < 10 sec.)	P_D Single	1.0	W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

ELECTRICAL CHARACTERISTICS ($T_J = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Breakdown Voltage, ($I_C = -10$ mAdc, $I_B = 0$)	$V_{(BR)CEO}$	−12	–	–	Vdc
Collector−Base Breakdown Voltage, ($I_C = -0.1$ mAdc, $I_E = 0$)	$V_{(BR)CBO}$	−12	–	–	Vdc
Emitter−Base Breakdown Voltage, ($I_E = -0.1$ mAdc, $I_C = 0$)	$V_{(BR)EBO}$	−5.0	–	–	Vdc
Collector Cutoff Current, ($V_{CB} = -12$ Vdc, $I_E = 0$)	I_{CBO}	–	−0.02	−0.1	μAdc
Emitter Cutoff Current, ($V_{CES} = -5.0$ Vdc, $I_E = 0$)	I_{EBO}	–	−0.03	−0.1	μAdc
ON CHARACTERISTICS					
DC Current Gain (Note 3) ($I_C = -10$ mA, $V_{CE} = -2.0$ V) ($I_C = -500$ mA, $V_{CE} = -2.0$ V) ($I_C = -1.0$ A, $V_{CE} = -2.0$ V)	h_{FE}	 200 100 90	 – – –	 – – –	
Collector−Emitter Saturation Voltage (Note 3) ($I_C = -0.05$ A, $I_B = -0.005$ A) (Note 4) ($I_C = -0.1$ A, $I_B = -0.002$ A) ($I_C = -0.1$ A, $I_B = -0.010$ A) ($I_C = -0.5$ A, $I_B = -0.050$ A) ($I_C = -1.0$ A, $I_B = -0.100$ A)	$V_{CE(sat)}$	 – – – – –	 −0.030 −0.080 −0.050 −0.200 −0.400	 −0.040 −0.100 −0.060 −0.225 −0.440	V
Base−Emitter Saturation Voltage (Note 3) ($I_C = -1.0$ A, $I_B = -0.01$ A)	$V_{BE(sat)}$	 –	 0.95	 −1.15	V
Base−Emitter Turn−on Voltage (Note 3) ($I_C = -2.0$ A, $V_{CE} = -3.0$ V)	$V_{BE(on)}$	 –	 −1.05	 −1.15	V
Input Capacitance ($V_{EB} = -0.5$ V, f = 1.0 MHz)	Cibo	–		50	pF
Output Capacitance ($V_{CB} = -3.0$ V, f = 1.0 MHz)	Cobo	–		20	pF

1. FR−4 @ 100 mm^2, 1 oz copper traces.
2. FR−4 @ 500 mm^2, 1 oz copper traces.
3. Pulsed Condition: Pulse Width = 300 μsec, Duty Cycle ≤ 2%.
4. Guaranteed by design but not tested.

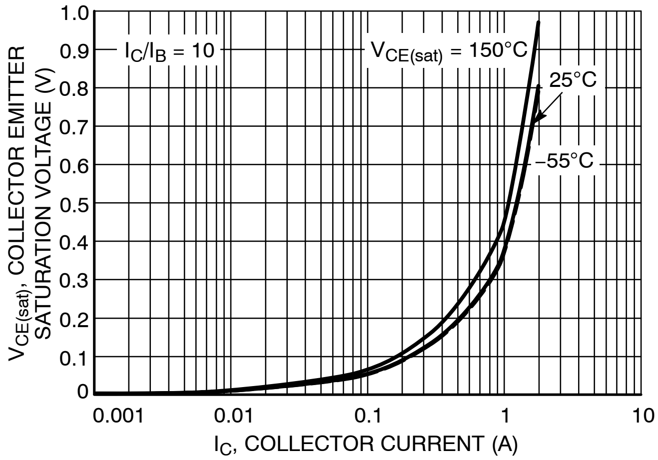


Figure 1. Collector Emitter Saturation Voltage vs. Collector Current

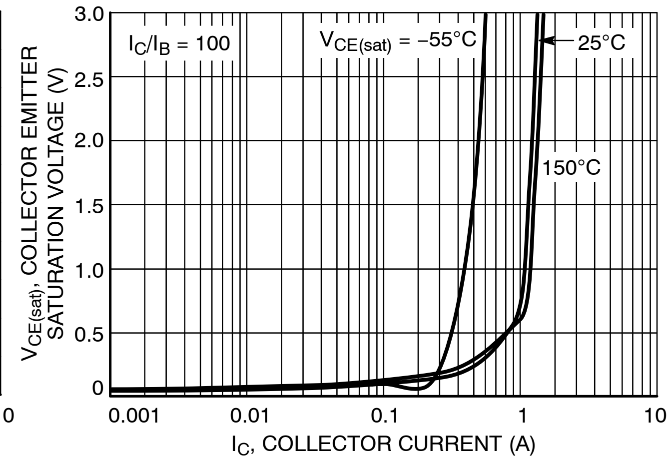


Figure 2. Collector Emitter Saturation Voltage vs. Collector Current

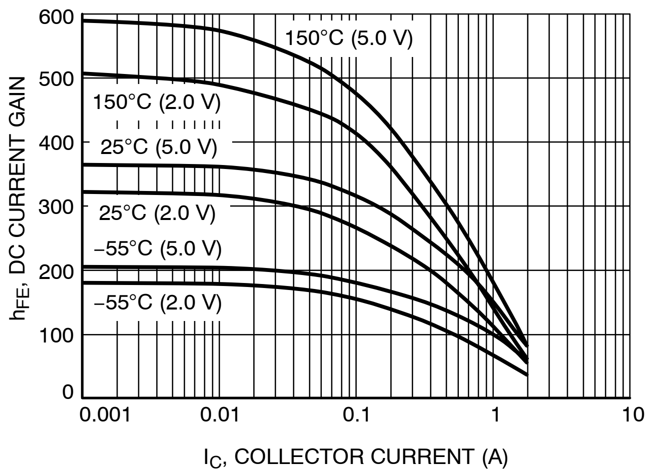


Figure 3. DC Current Gain vs. Collector Current

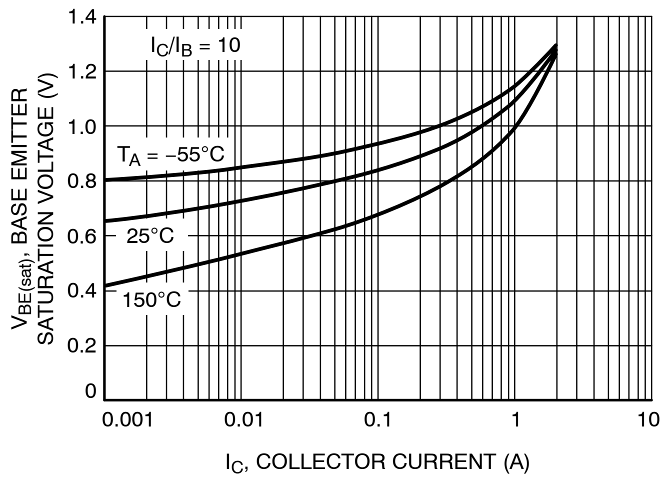


Figure 4. Base Emitter Saturation Voltage vs. Collector Current

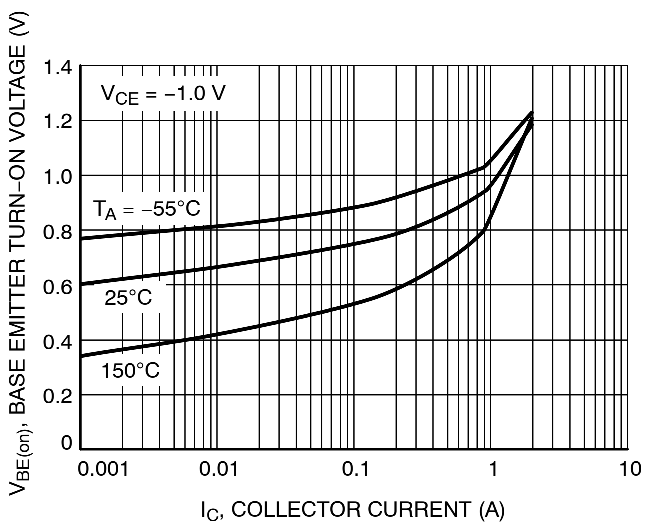


Figure 5. Base Emitter Turn−On Voltage vs. Collector Current

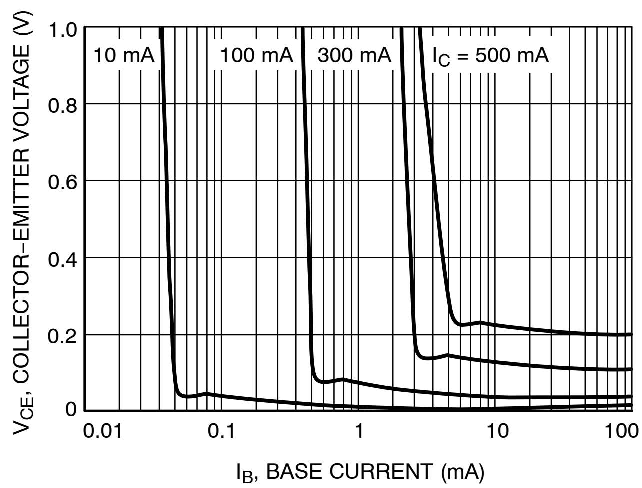


Figure 6. Saturation Region

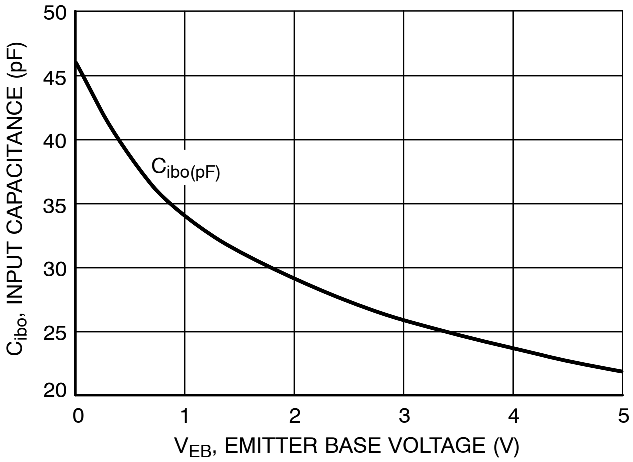


Figure 7. Input Capacitance

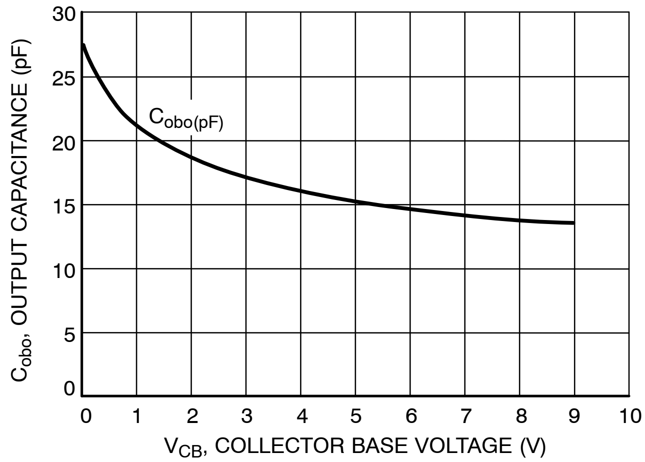
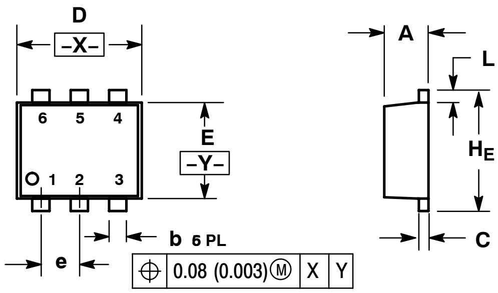


Figure 8. Output Capacitance

PACKAGE DIMENSIONS

SOT−563, 6 LEAD
CASE 463A−01
ISSUE F

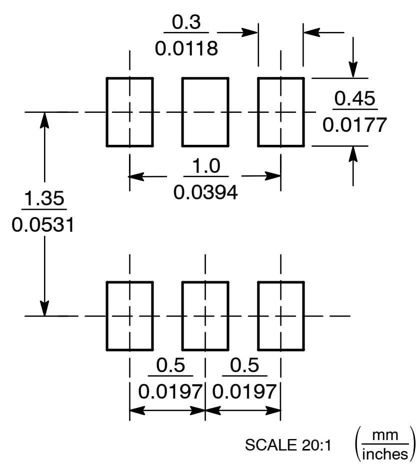


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS			INCHES		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	0.50	0.55	0.60	0.020	0.021	0.023
b	0.17	0.22	0.27	0.007	0.009	0.011
C	0.08	0.12	0.18	0.003	0.005	0.007
D	1.50	1.60	1.70	0.059	0.062	0.066
E	1.10	1.20	1.30	0.043	0.047	0.051
e	0.5 BSC			0.02 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
H_E	1.50	1.60	1.70	0.059	0.062	0.066

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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