LV8811G, LV8813G

Motor Driver, 3-Phase, PWM, Full-Wave, BLDC

ON Semiconductor®
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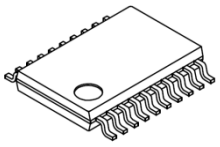
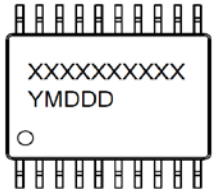


20-pin TSSOP with exposed pad
CASE 948AZ

MARKING DIAGRAM



XXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

ORDERING INFORMATION

Ordering Code:
LV8811G-AH
LV8813G-AH

Package
TSSOP20J
(Pb-Free / Halogen Free)

Shipping (Qty / packing)
2000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF

Overview

The LV8811G, LV8813G are a 3-phase BLDC motors driver which are controlled by single Hall sensor. A 180 degrees sinusoidal driving method is adopted and the IC can control motor with low vibration and the low noise. In addition, lead-angle adjustment is possible by external pins. Lead-angle value and lead-angle slant can be adjusted independently. Thus, the device can be driven by high efficiency and low noise with various motors. The power element to drive a motor is built-in and contributes to high efficiency by low on resistance (0.5 Ω). The Hall sensor bias driver is equipped, and a Hall IC is supported as well. As a method of the rotary speed control of the motor, direct-PWM pulse input or DC-voltage input can be chosen.

Features

·3-phase full wave (sinusoidal) drive
·Any practical combination of slot and pole can be handled. (e.g. 3S2P, 3S4P, 6S4P, 6S8P, 12S8P, 9S12P and so on)
·Built-in power FETs (P-MOS/N-MOS)
·Speed control function by direct PWM or DC voltage input
·Minimum input PWM duty cycle can be configured by voltage input
·Soft start-up function and soft shutdown function
·Soft PWM duty cycle transitions
·Built-in current limit circuit and thermal protection circuit
·Regulated voltage output pin for Hall sensor bias
·Built-in locked rotor protection and auto recovery circuit
·FG signal output
·Dynamic lead angle adjustment with respect to rotational speed
·Lead-angle control parameters can be configured by voltage inputs.

Typical Applications

·Refrigerator
·PC
·Games

BLOCK DIAGRAM

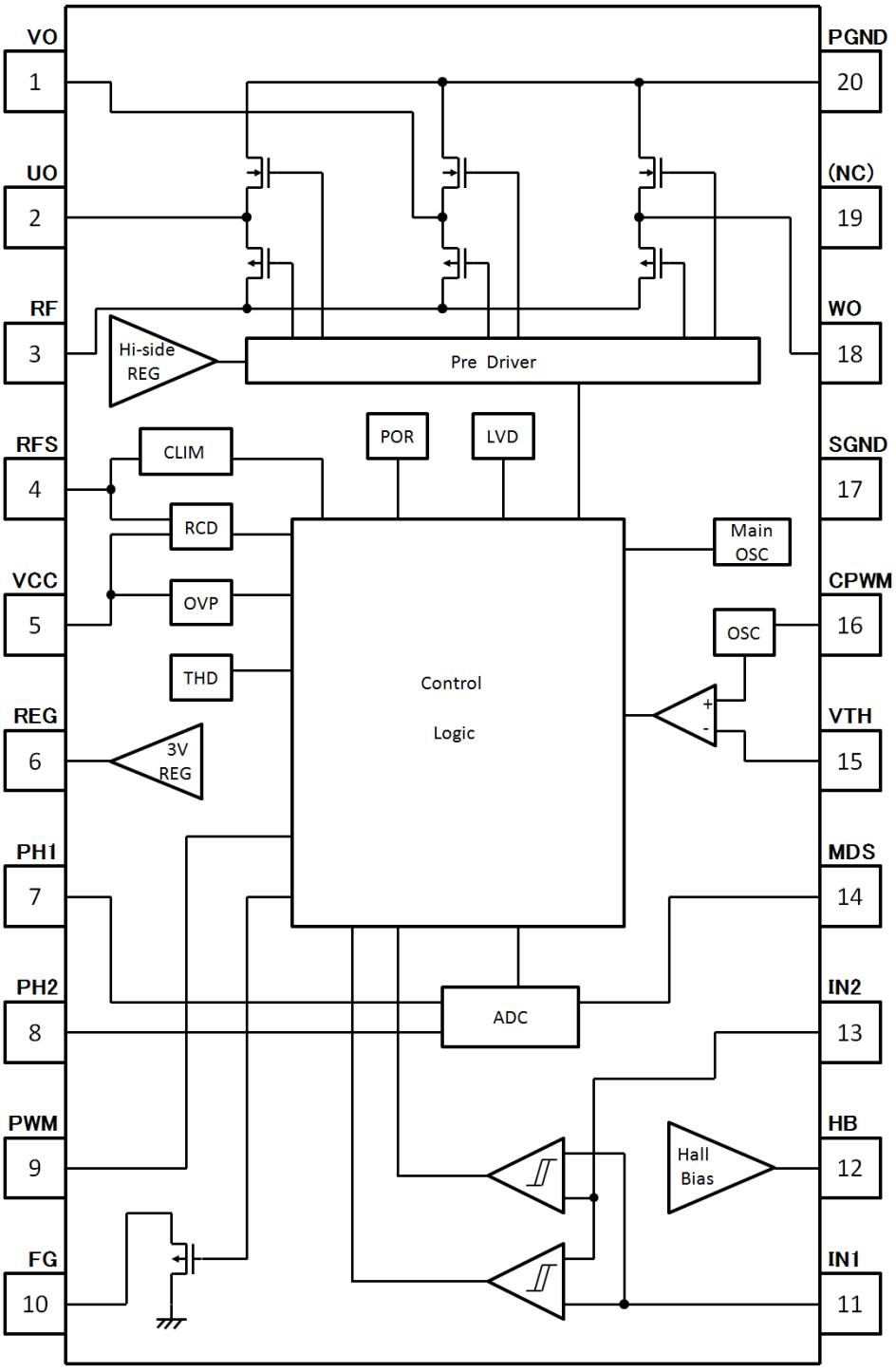


Figure 1. LV8811G, LV8813G Block Diagram

APPLICATION CIRCUIT DIAGRAM

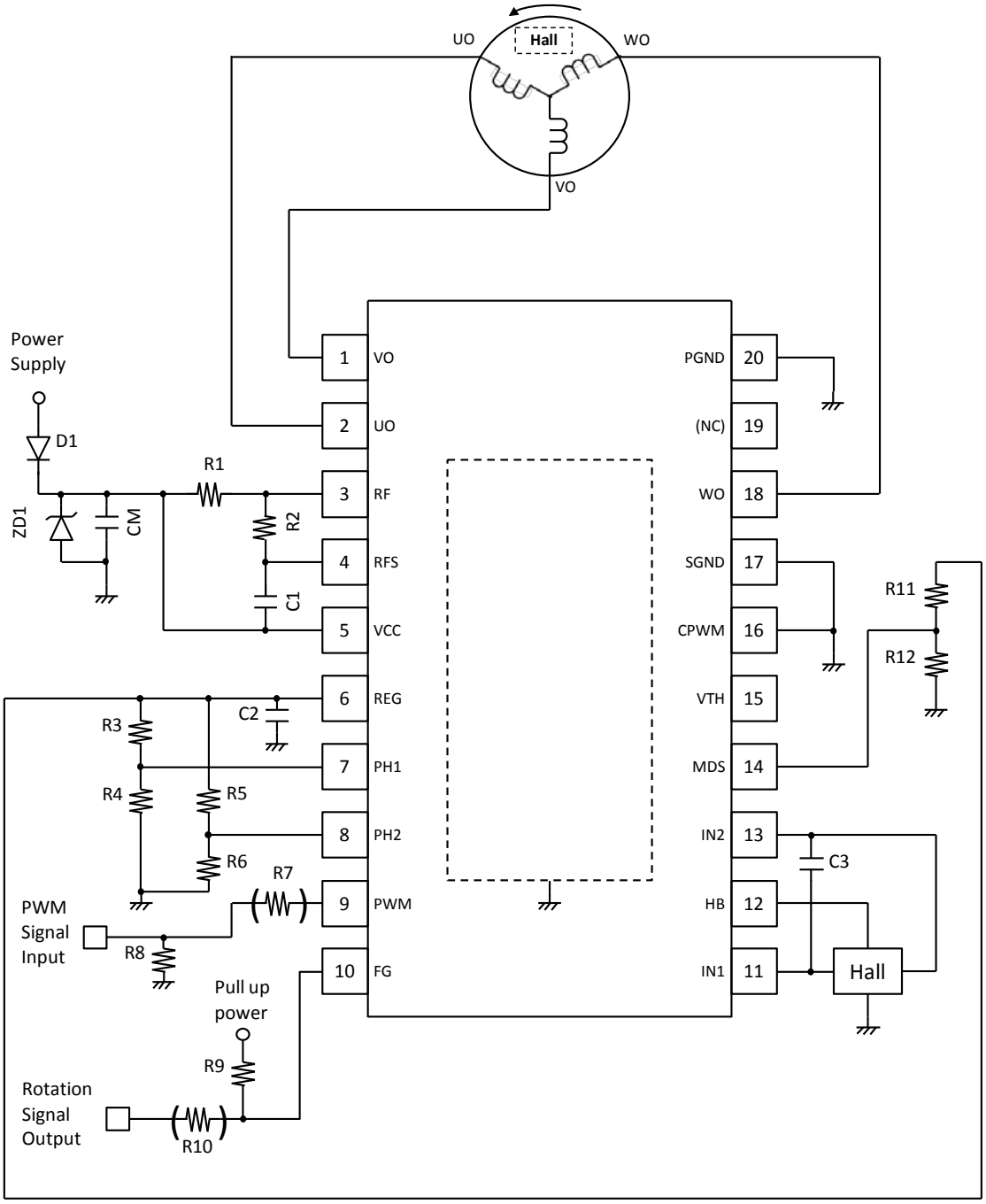


Figure 2. Three-phase BLDC Motor Drive with LV8811G, LV8813G using One Hall Sensor

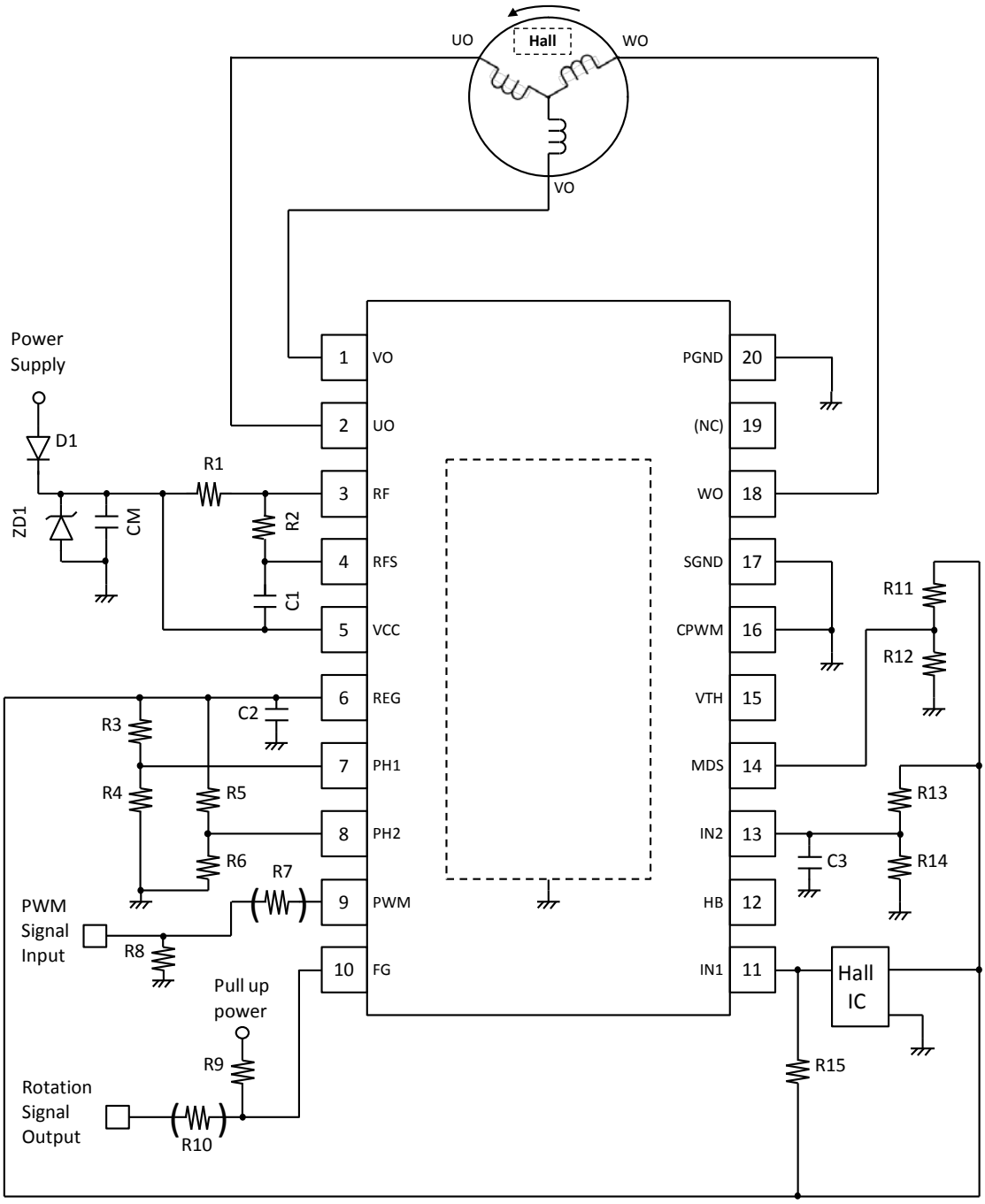


Figure 3. Three-phase BLDC Motor Drive with LV8811G, LV8813G using One Hall IC

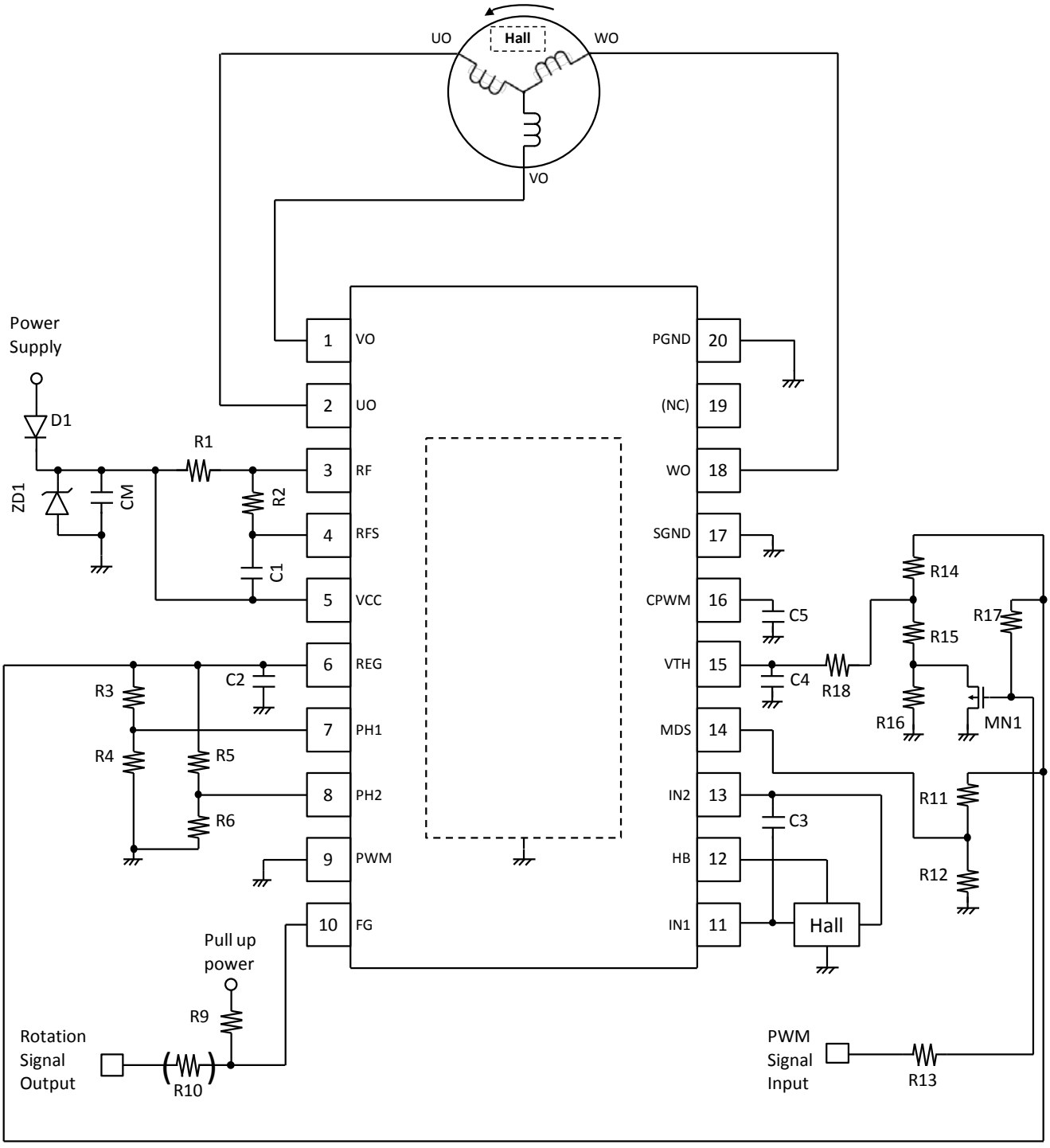


Figure 4. Three-phase BLDC Motor Drive with LV8811G, LV8813G using input PWM to DC conversion for speed control

EXAMPLE COMPONENT VALUE

Device	Value	Device	Value
D1	MBRA340T3G (ON semi)	R5	0 to 50kΩ
ZD1	MNSZ5247BT1G (ON semi)	R6	50k to 0Ω
		R7	1kΩ
CM	4.7μF	R8	NC
C1	1500pF	R9	1k to 10kΩ
C2	1μF	R10	1kΩ
C3	0.1μF	R11	0 to 50kΩ
C4	1μF	R12	50k to 0Ω
C5	330pF	R13	10kΩ
		R14	30kΩ
R1	0.22Ω // 0.22Ω (0.5W)	R15	7.5kΩ
R2	1kΩ	R16	62kΩ
R3	0 to 50kΩ	R17	68kΩ
R4	50k to 0Ω	R18	1kΩ

PIN ASSIGNMENT

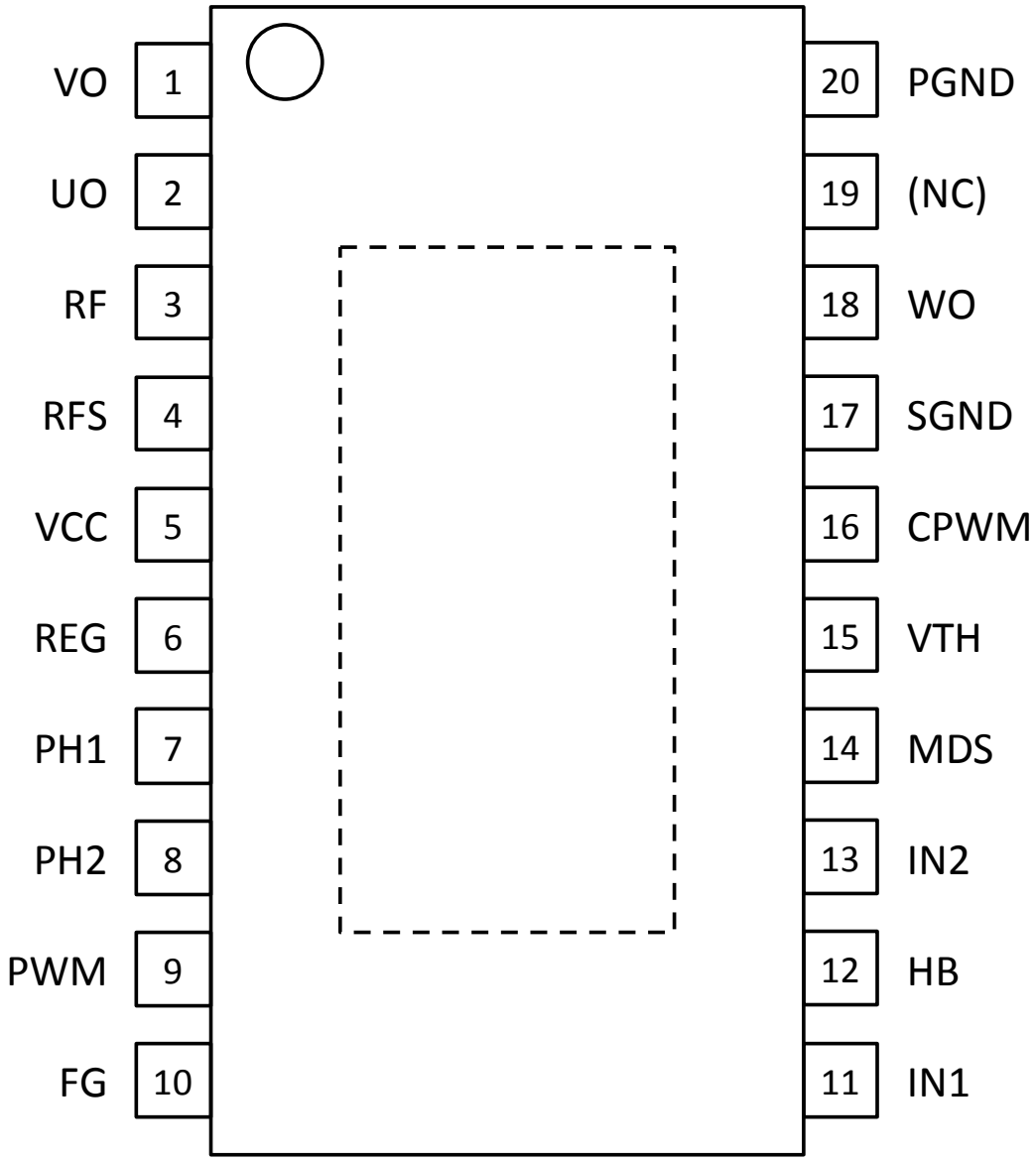


Figure 5. LV8811G, LV8813G Pin Assignment

LV8811G VS LV8813G COMPARISION

ASSUME APPLICATION

-LV8811G : Wide operation supply voltage range. Suitable for small-size fans.
-LV8813G : Stable start-up even with a large load. Suitable for large-size fans.

DIFFERENT CHARACTERISTICS

	LV8811G	LV8813G	Comment	Reference page
VCC/RF operating Supply voltage range	3.6V to 16V	6.0V to 16V	LV8811G has a wide operation voltage range. LV8813G has a different Vcc lower limit to support large-size fan.	10
Alignment duty cycle	6%- >5%-> 20%->15%	50%->25%	LV8813G has stronger alignment to secure the start-up of large-size fans.	20
Alignment time	0.8ms	1.0s	LV8813G has longer alignment time to secure the start-up of large-size fans.	10, 20, 23,25
Lock detection time	0.33s	0.77s	LV8813G has longer detection time to prevent false Lock detection on large-size fans at the start-up.	10, 23, 25
Lock-Stop Release Time	5.8s	5.4s	This characteristic is different due to a different Lock detection time.	23, 25
Lock/Release time ratio	1:5	1:3		

PIN FUNCTION DISCRIPTION

Pin No.	Pin Name	Description
1	VO	V-phase output pin
2	UO	U-phase output pin
3	RF	Inverter power supply and Motor current sense resistor pin
4	RFS	Motor Current Sense
5	VCC	Power supply pin
6	REG	Internal regulator output pin
7	PH1	Lead-angle adjustment pin 1
8	PH2	Lead-angle adjustment pin 2
9	PWM	Speed reference input PWM pin
10	FG	Motor speed feedback output pin
11	IN1	Hall sensor input pin 1
12	HB	Hall sensor bias output pin
13	IN2	Hall sensor input pin 2
14	MDS	Minimum output PWM duty cycle setting pin
15	VTH	Speed reference input DC voltage pin
16	CPWM	PWM clock frequency control pin
17	SGND	System ground pin
18	WO	W-phase output pin
19	NC	No connection
20	PGND	Power ground pin

MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Maximum supply voltage (Note2)	VCC_{MAX}	20	V
Maximum output voltage (Note3)	$VOUT_{MAX}$	20	V
Maximum output current (Note3, Note4)	$IOUT_{MAX}$	2.0	A
REG pin maximum load current	$IREG_{MAX}$	20	mA
HB pin maximum load current	IHB_{MAX}	10	mA
PWM pin maximum input voltage	$VPWM_{MAX}$	6	V
FG pin maximum voltage	VFG_{MAX}	17	V
Input pins maximum voltage (Note5)	(Note 6)	3.6	V
Allowable Power Dissipation (Note7)	Pd_{MAX}	2.5	W
Storage Temperature	T_{stg}	−55 to 150	°C
Junction Temperature	$T_{J_{MAX}}$	150	°C
Moisture Sensitivity Level (MSL) (Note8)	MSL	3	-
Lead Temperature Soldering Pb-Free Versions (30sec or less) (Note 9)	T_{SLD}	255	°C
ESD Human body Model : HBM (Note10)	ESD_{HBM}	±2000	V

1. Stresses exceeding those listed in the Maximum Rating table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. VCC supply pins are VCC(5pin), RF(3pin), and RFS(4pin).
3. Motor power supply pins are UO(2pin), VO(1pin), and WO(18pin).
4. $IOUT_{MAX}$ is the peak value of the motor supply current.
5. Input pins are PH1(7pin), PH2(8pin), IN1(11pin), IN2(13pin), MDS(14pin), VTH(15pin), and CPWM(16pin).
6. Pin : Symbol PH1:$VPH1_{MAX}$, PH2:$VPH2_{MAX}$, IN1:$VIN1_{MAX}$, IN2:$VIN2_{MAX}$, MDS:$VMDS_{MAX}$, VTH:$VVTH_{MAX}$, CPWM:$VCPWM_{MAX}$
7. Specified circuit board : 57.0mm×57.0mm×1.6mm, glass epoxy 2-layer board. It has 1 oz copper traces on top and bottom of the board. Please refer to Thermal Test Conditions of page 32.
8. Moisture Sensitivity Level (MSL): 3 per IPC/JEDEC standard: J-STD-020A
9. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D http://www.onsemi.com/pub_link/Collateral/SOLDERRM-D.PDF
10. ESD Human Body Model is based on JEDEC standard: JESD22-A114

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient (Note7)	$R_{\theta JA}$	50.0	°C/W
Thermal Resistance, Junction-to-Case (Top) (Note7)	$R_{\Psi JT}$	15.5	°C/W

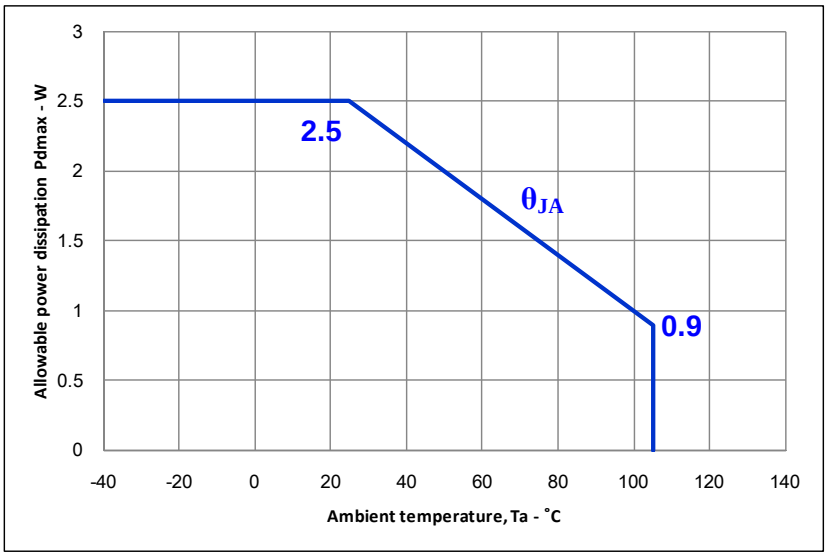


Figure 6. Power Dissipation vs Ambient Temperature Characteristic

RECOMMENDED OPERATING RANGES (Note11)

Parameter	Symbol	Ratings	Unit
VCC supply voltage Range at LV8811G (Note2)	VCC_{OP}	3.6 to 16.0	V
VCC supply voltage Range at LV8813G (Note2)		6.0 to 16.0	V
PWM input frequency range	f_{PWM}	20 to 50	kHz
PWM input duty cycle range	D_{PWM}	0 to 100	%
PWM input voltage range	V_{PWM}	0 to 5	V
IN1 input voltage range	V_{IN1}	0 to V_{REG}	V
IN2 input voltage range	V_{IN2}	0.3 to 1.8	V
Control input Voltage Range (Note12)	(Note 13)	0 to V_{REG}	V
Ambient Temperature	T_A	−40 to 105	ºC

11. Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
12. Control input pins are PH1, PH2, MDS, and VTH
13. Pin : Symbol PH1:V_{PH1}, PH2:V_{PH2}, MDS:V_{MDS}, VTH:V_{VTH}

ELECTRICAL CHARACTERISTICS

TA=25ºC, VCC_{OP} = 12V UNLESS OTHERWISE NOTED. (NOTE 14)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Circuit Current						
Supply Current	ICC0	PWM = 3V, CPWM=0V, I_O=0A		4.5	7.0	mA
Protection (Note15)						
Over Current Detection Voltage	VTH_{CLM}	The voltage between VCC - RF	0.162	0.180	0.198	V
Over Voltage Detection Voltage	VTH_{OVP}	VCC pin, Guaranteed by design	19	20		V
Over Voltage Detection Hysteresis	ΔVTH_{OVP}	VCC pin, Guaranteed by design		2		V
Lock Detection Time	T_{LD}	Case of the LV8811G	0.23	0.32	0.41	S
		Case of the LV8813G	0.55	0.76	0.97	S
Lock Protection Time	T_{LP}	Case of the LV8811G	4.15	5.68	7.21	S
		Case of the LV8813G	3.82	5.23	6.64	S
Thermal Protection Detection Temperature	T_{THP}	Guaranteed by design	150	180		˚C
Thermal Protection Detection Hysteresis	ΔT_{THP}	Guaranteed by design		15		˚C
Regulator						
REG Pin Output Voltage	V_{REG}		2.7	3.0	3.3	V
Output						
UO/VO/WO Output Resistance	$ROUT_{ON}$	I_O=0.8A, High-side + Low-side		0.5	0.65	Ω
FG Output (Note16)						
FG Pin Low Level Output Voltage	V_{FGL}	I_{FG}=5mA			0.3	V
FG Pin Leak Current	I_{FGLK}	V_{FG}=16V			1	μA
Hall Bias & Hall Signal Input						
HB Pin Output Voltage	V_{HB}	I_{HB}=5mA	1.06	1.18	1.30	V
IN1/IN2 Input Current	I_H				1	μA
Hall Signal Input Hysteresis	ΔV_H	Guaranteed by design		+/-10		mV

Continued on next page.

Continued from preceding page.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
PWM Input						
PWM Pin Low Level Input Voltage	V_{PWML}		0		0.6	V
PWM Pin High Level Input Voltage	V_{PWMH}		2.3		5.5	V
PWM On Time	T_{PWMON}	Guaranteed by design	200			ns
PWM Off Time	T_{PWMOFF}	Guaranteed by design	200			ns
CPWM Input						
CPWM Minimum Output Ratio (Note17)	$\frac{V_{CPWML}}{V_{REG}} \times 100$		16	18	20	%
CPWM Maximum Output Ratio (Note17)	$\frac{V_{CPWMH}}{V_{REG}} \times 100$		65	67	69	%
CPWM Source Current	I_{CPWMSO}	V_{CPWM}=1.3V	17	29	41	μA
CPWM Sink Current	I_{CPWMSI}	V_{CPWM}=1.3V	-41	-29	-17	μA

14. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
15. Refer to the protection circuit explanation in the function description. Refer to page 23.
16. For FG output pin, it is recommended to connect pull-up resistor between the pin and power supply of the controller.
17. V_{CPWMH} and V_{CPWML} are peak voltage of triangle wave in CPWM pin.

TYPICAL CHARACTERISTICS

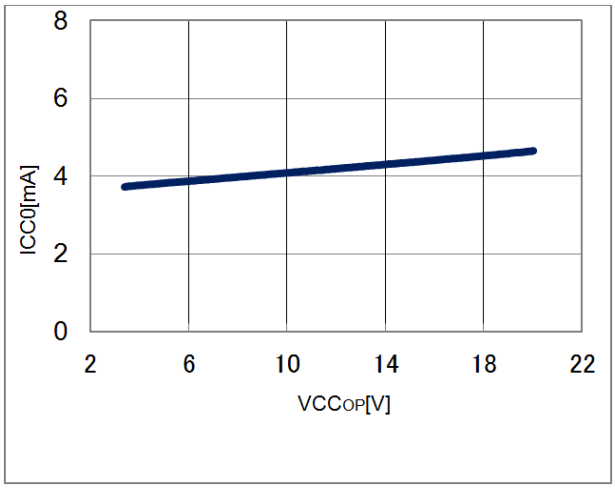


Figure 7. Supply current vs VCC voltage

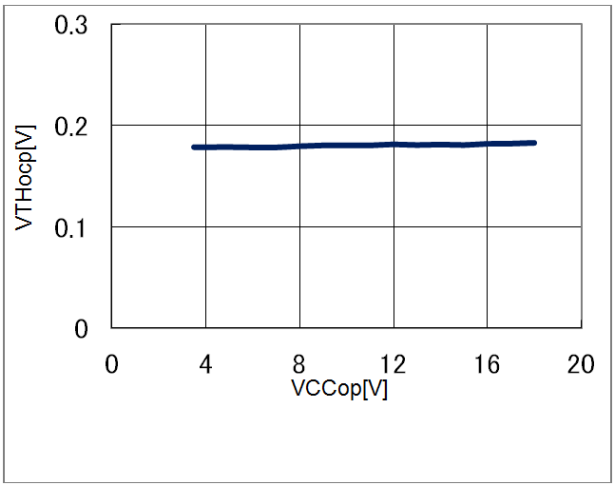


Figure 10. Current limiter detection voltage vs VCC voltage

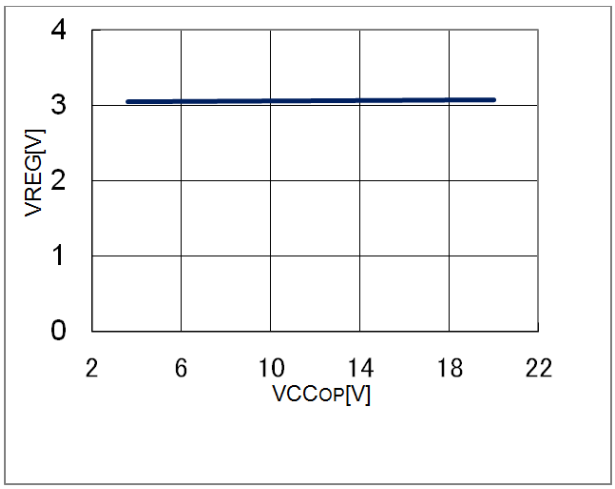


Figure 8. V_{REG} output voltage vs VCC voltage

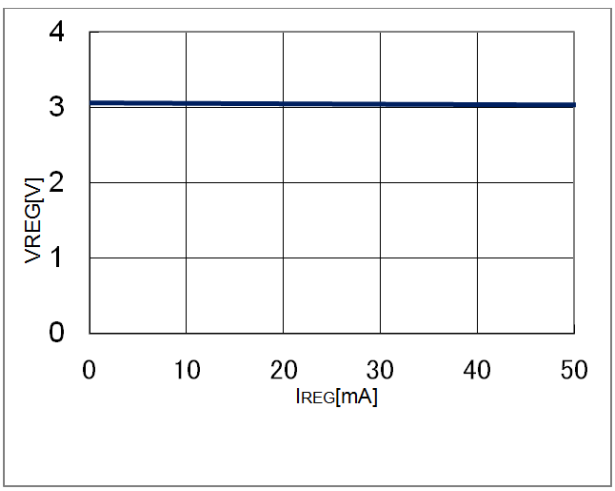


Figure 11. V_{REG} output voltage vs REG load current

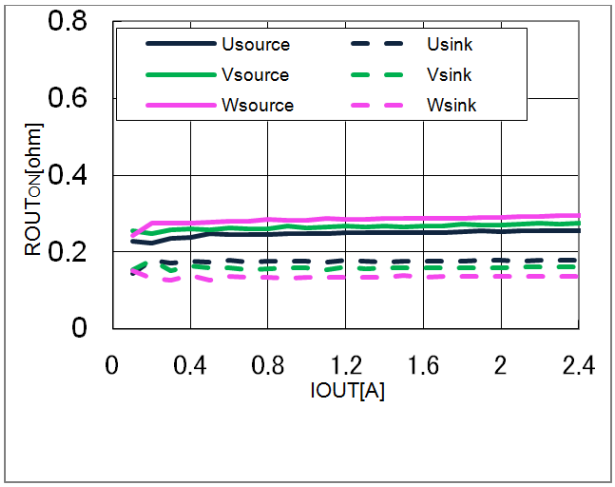


Figure 9. Output ON resistance vs Output current

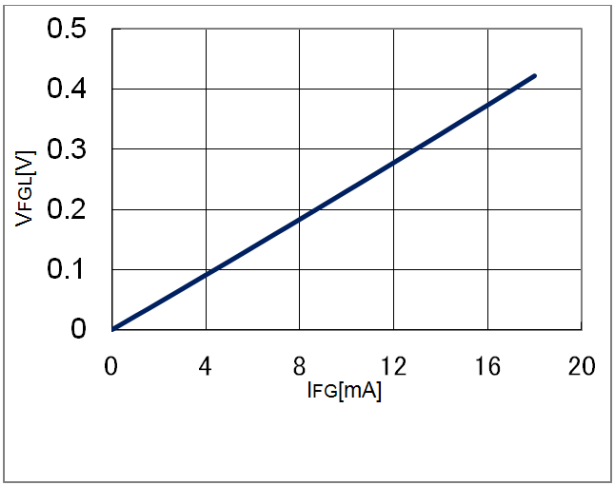


Figure 12. FG output voltage vs FG input current

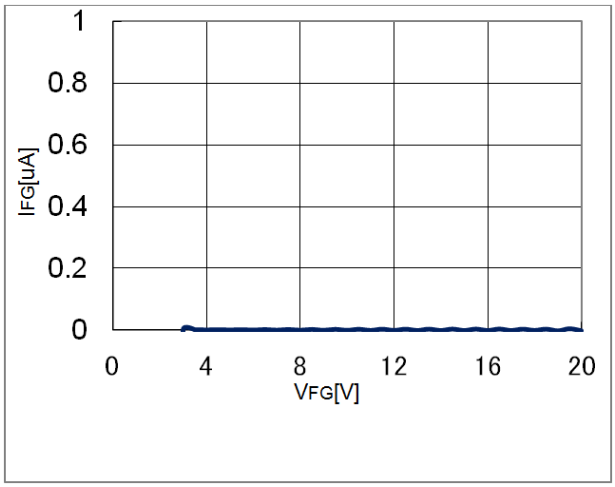


Figure 13. FG leakage current vs FG input voltage

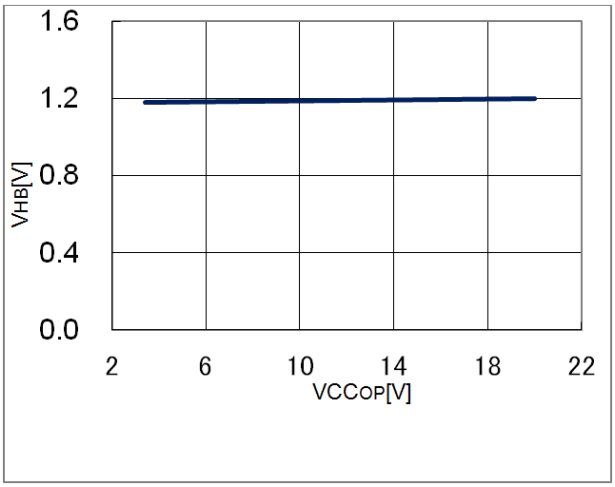


Figure 16. V_{HB} output voltage vs VCC voltage

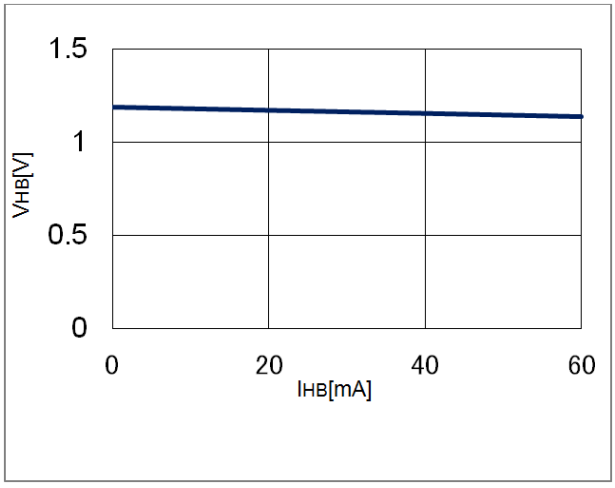


Figure 14. V_{HB} output voltage vs HB load current

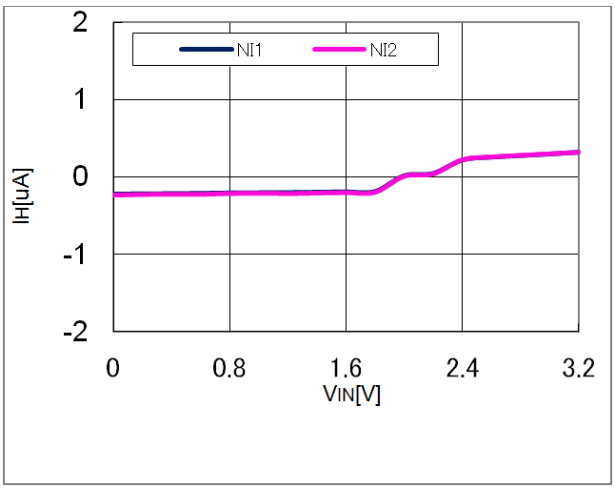


Figure 17. IN1/IN2 input current vs IN1/IN2 input voltage

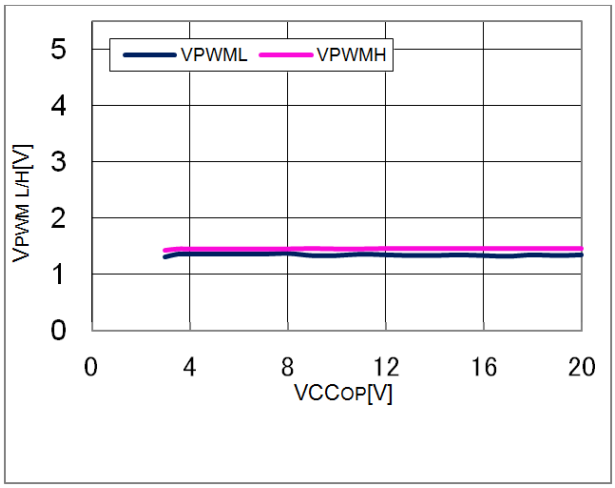


Figure 15. PWM threshold voltage vs VCC voltage

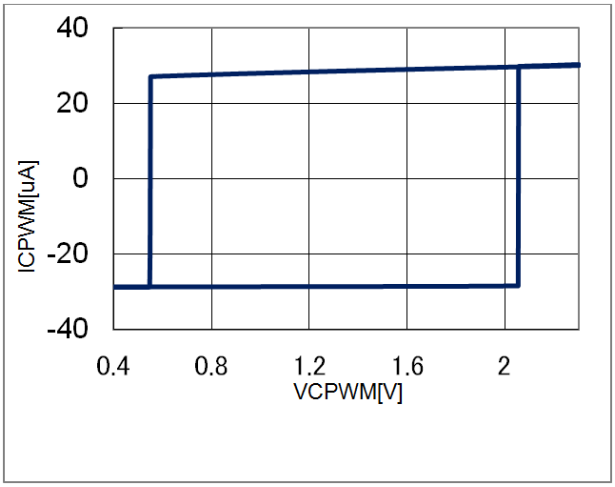


Figure 18. CPWM charge/discharge current

Functional Description

POWER SUPPLY PINS (VCC, RF)

RF is output power supply whereas VCC is other circuit supply. The RF pin supplies large current to built-in power MOS FTEs. (Figure 23)

*Please refer to page.*15 'Motor Current Sense Resistor Pin (RF)'* about the CLM sense resistance of RF terminal.

GND PIN (SGND, PGND)

PGND is power ground whereas SGND is other circuit ground. Since PGND has to tolerate surge of current, separate it from the SGND as far away as possible and connect it point-to-point to the ground side of the capacitor (CM) between power supply and ground.

Internal 3.0V Voltage Regulator Pin (REG)

An internal 3.0V voltage regulator acts a power source for internal logic, oscillator, and protection circuits. When MDS and PH1 and PH2 are used, it is recommended that application circuits are made using this output. In addition, the application circuit of VTH is same, too. The maximum load current of REG is 10mA. Warn not to exceed this. Place capacity of 1uF degree and the 0.1uF degree in the close this pin. (Figure 19)

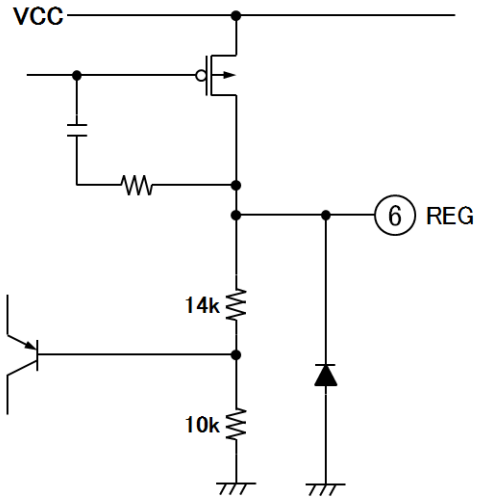


Figure 19. Equivalent circuit of REG

ROTATIONAL SIGNAL PIN (FG)

Frequency of the FG output represents the motor's electrical rotational speed (the same rectangular waves as the UO). It is an open drain output. Recommended pull up resistor value is 1kΩ to 10kΩ. Leave the pin open when not in use. (Figure 20)

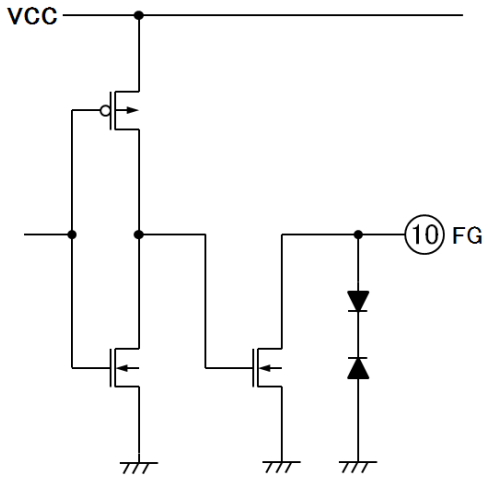


Figure 20. Equivalent circuit of FG

MOTOR DRIVE OUTPUT PINS (UO, VO, WO)

These pins are output of built-in three-phase MOSFET based inverter that drives the motor. Each leg of the inverter is having high side P-MOSFET and low side N-MOSFET. (Figure 21)

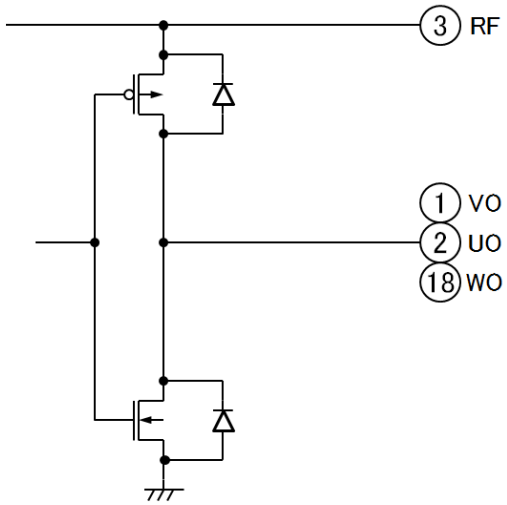


Figure 21. Equivalent circuit of U/V/W

HALL-SENSOR BIAS OUTPUT PIN (HB)

The LV811G, LV8813G provides a bias regulator output (1.18V typ.) for a hall sensor. It is recommended that this output used only for hall sensor bias.

HALL-SENSOR INPUT PINS (IN1, IN2)

Differential output signals of a Hall sensor are connected to IN1 and IN2 individually. Its polarity is determined by a combination of the number of slot and poles. (Figure 29)

It is recommended to add 0.1uF capacitor between them to filter system noise.

Topologies, in the case of a Hall IC, are shown in Figure 30 on page18. The topology (including polarity) is also determined by the combination of the number of slot and poles.

When the pin IN1 is connected to the output of the Hall IC, the pin IN2 must be kept in the middle level of the Hall IC power supply voltage. When the pin IN2 is connected to the output of the Hall IC, the pin IN1 must be kept in the middle level of the Hall IC power supply voltage. Because of the input circuit (Figure 22), the input voltage of IN2 must be higher than 0.3V. Therefore, The resistance ratio must be decided so that IN2 voltage is higher than 0.3V. (Figure 30)
Regarding the polarity of a Hall sensor and IC, refer *'Rotation Direction'* on page*18*.

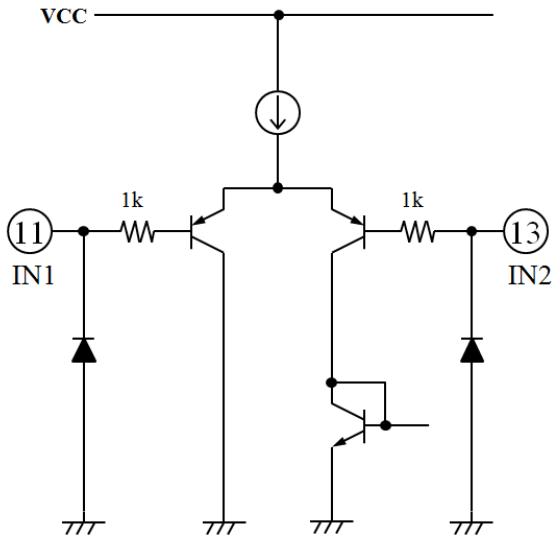


Figure 22 Equivalent circuit of IN1, IN2

MOTOR CURRENT SENSE RESISTOR PIN (RF)
This is also the power supply pin for the built-in power inverter. Voltage across the sense resistor represents the motor current and is compared against the internal VTH_{OVC} (0.18Vtyp.) for setting the over-current limiter (CLM). (Figure 23)

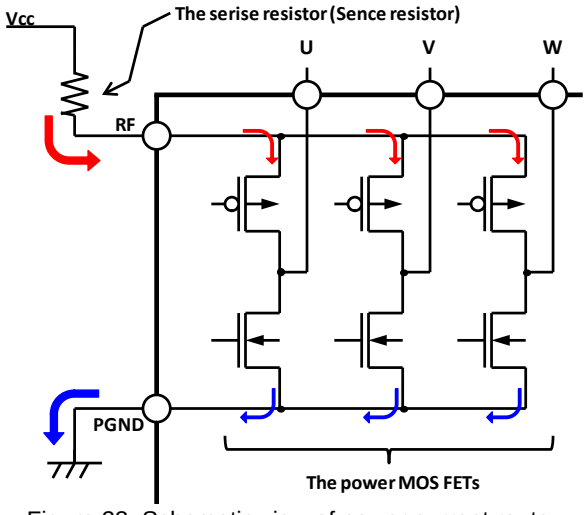


Figure 23. Schematic view of power current route

The sense resistor value is calculated as follows.

$$\text{Sense Resistor}[\Omega] = \frac{VTH_{CLM}[V]}{I_{CLM}[A]}$$

For example, to set the CLM current threshold at 1.5A, the sense resistor value is

$$\text{Sense Resistor} = \frac{0.18(\text{typ})}{1.5}$$
$$\text{Res} = 0.12[\Omega]$$

MOTOR CURRENT SENSE PIN (RFS)
This pin reads voltage across the series sense resistor and compares with internal VTH_{CLM}. When the measured voltage exceeds VTH_{CLM}, CLM is triggered and when it falls below VTH_{CLM}, the LV8811G, LV8813G exits from the CLM mode. A series RC filter is recommended to avoid false detection due to switching noise. (Figure 24)

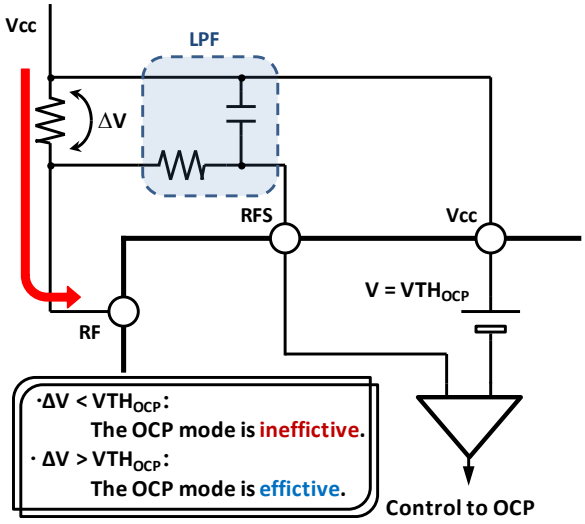


Figure 24. Schematic view of the CLM circuit

COMMAND INPUT (PWM)

This pin reads the duty cycle of the PWM pulse and controls rotational speed. The PWM input signal level is supported from 2.5V to 5V. The combination with the rotational speed control by DC voltage, is impossible. When the pin is not used, it must be connected to ground. The minimum pulse width is 200ns. (Figure 25)

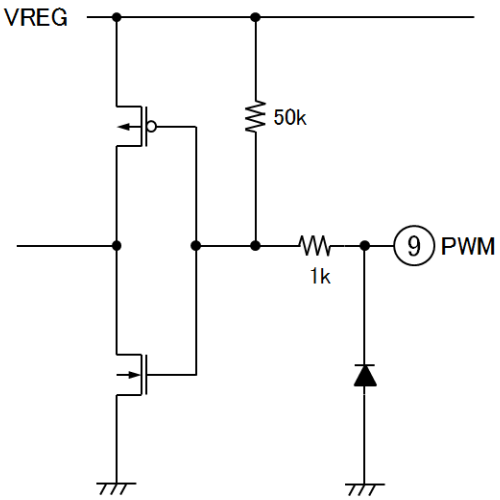


Figure 25. Equivalent circuit of PWM

MINIMUM DUTY CYCLE SETTING PIN (MDS)

The too small duty cycle of the input PWM can be blanked out. The threshold of the minimum duty cycle is configurable. The DC voltage level applied to this pin is converted to this threshold. The voltage is fetched right after the power-on-reset. Because the internal conversion circuit works inside REG power rail, it is recommended that the MDS voltage is made from V_{REG}. This pin is also used for setting of FG frequency. Refer *'Parameter Setting by Constant Voltage'* on page *28*, and *'Setting Minimum PWM Duty Cycle'* on page *29*.

LEAD-ANGLE SETTING PIN (PH1, PH2)

LV8811G, LV8813G provides the dynamic lead angle adjustment. To match the motor characteristics, the base angle and change ratio with respect to the rotation speed can be configured. The DC voltage levels applied to these pins are converted to the lead angle parameter. The voltages are fetched right after the power-on-reset. Because the internal conversion circuit works inside REG power rail, it is recommended that the PH1 and PH2 voltages are made from V_{REG}. Refer *'Parameter Setting by Constant Voltage'* on page *28*, and *'Setting Lead Angle'* on page *30*.

PWM FREQUENCY SETTING PIN (CPWM)

When rotational speed is controlled with the DC voltage, this pin is used. The frequency of the triangle wave which the pin generates at external capacity can be changed. The frequency of this triangle wave equals frequency of the PWM control that the output works. The relations between the external capacitor and frequency are shown in the next equation.

PWM Frequency f_{PWM} [Hz] is,

$$f_{PWM} = \frac{I_{CPWMSI/O}[A]}{2 \times (V_{CPWMH} - V_{CPWML})[V] \times C_{PWM}[pF]}$$

Where,

$I_{CPWMSI/O} = I_{CPWMSO} = -I_{CPWMSI} : 29[uA](typ.)$
Charge/discharge current

V_{CPWMH}: 2.01[V](typ.) Upper peak voltage of CPWM triangle waveform. 67% of 3V V_{REG}

V_{CPWML}: 0.54[V](typ.) Lower peak voltage of CPWM triangle waveform. 18% of 3V V_{REG}

For example, the capacitance of CPWM, to make the PWM frequency 30kHz, can be determined by the followings

$$30k = \frac{29u}{2.94 \times C_{PWM}}$$

$$C_{PWM} \cong 330[pF]$$

C_{PWM} decides output PWM frequency. Thus, this value must choose appropriately. The range from 220pF to 330pF is recommended. CPWM is represented C_5 in the application circuit diagram, Figure 4 on page *5*.

The combination with the rotational speed control by PWM is impossible. When this pin is not used, it must be connected to GND. Refer *'PWM duty CYCLE control by analog voltage'* on page *26*. (Figure 26)

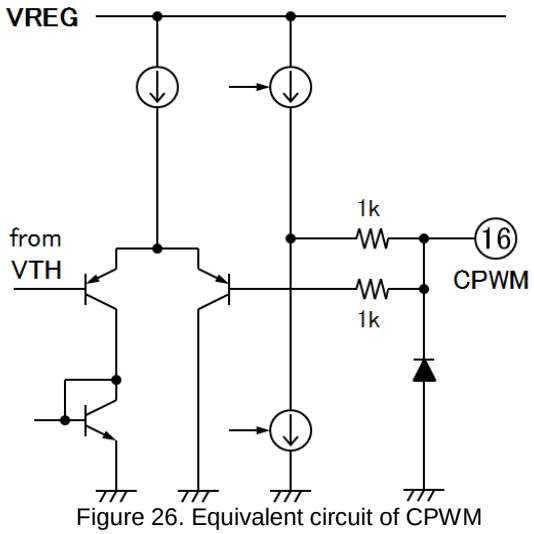


Figure 26. Equivalent circuit of CPWM

ROTATIONAL CONTROL PIN BY DC VOLTAGE (VTH)

This pin reads the input DC voltage and controls rotational speed. The VTH voltage is compared with the CPWM triangle wave with an internal comparator and generates PWM pulse and controls rotational speed with frequency and duty cycle of this pulse.
If the external control signal is the pulse type, it should be flattening by the filter and be shifted to suitable level. The external circuit example is shown in Figure 4.

VTH input level flatten by the filter is calculated in the following equation.

$$V_{VTH} = V_{REG} \times \left\{ \frac{R_{15} + R_{16}}{R_A} - \frac{R_{14} \times R_{16}}{R_A \times R_B} \times \frac{D_{PWM}}{100} \right\}$$

Where

$R_A = R_{14} + R_{15} + R_{16}$
$R_B = R_{14} + R_{15}$
$V_{VTH} =$ VTH input level

This calculation is justified by the condition that Rds of MN1 << R_{16}. So, a large value of resistor should be selected to R_{16}.

For example, when the input PWM duty cycle is set in 50%, can be determined by follows.

$$V_{VTH} = 3[V] \times (0.698 - 0.498 \times \frac{50[\%]}{100})$$
$$V_{VTH} = 1.35[V]$$

Where

R_{14}=7.5[kΩ], R_{15}=30[kΩ], R_{16}=62[kΩ]

The cut-off frequency fc by C_4 and R_{18} is calculated in the following equation.

$$f_c = \frac{1}{2\pi \times C_4 \times R_{18}}$$

The actual value of C_4 or R_{18} is better to select more than 50 times the above calculation value to be flatten thoroughly. Furthermore, it is better to do it by the value of C_3 because of the effect of input impedance at VTH pin.

If the external control signal is the DC type, it inputs into direct VTH pin. However, It is recommended that the filter (C_4 and R_{18}) is kept because rid of the influence of the noise.

The CPWM amplitude is decided by VREF. Thus, VTH recommends that it is made from V_{REG}. The combination with the rotational speed control by PWM is impossible. When the pin is not used, it must be OPEN. Refer *'PWM duty CYCLE control by analog voltage'* on page *26*. (Figure 27)

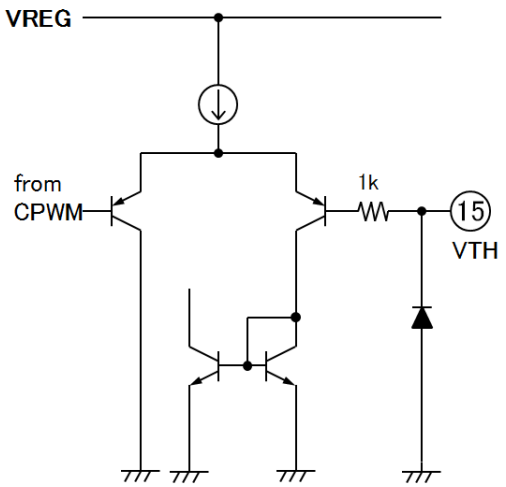


Figure 27. Equivalent circuit of VTH

NC PIN (NC)

This pin is not connection to the internal circuit.

DETAILED DESCRIPTION

As for all numerical value used in this description, the design value or the typical value is used.

ROTATION DIRECTION

The motor type can be categorized into two groups as 3S2P and 3S4P. (S: Slot, P: Pole). The 3S2P group contains 3S2P, 6S4P and 12S8P, for instance, and 3S4P groups contains 3S4P, 6S8P and 9S12P. The rotate direction of 3S2P group is CW, that of 3S4P group is CCW. The direction can be changed by exchanging connection between U and W, in the case where the hall sensor is between U coil and W coil. (Figure 28)

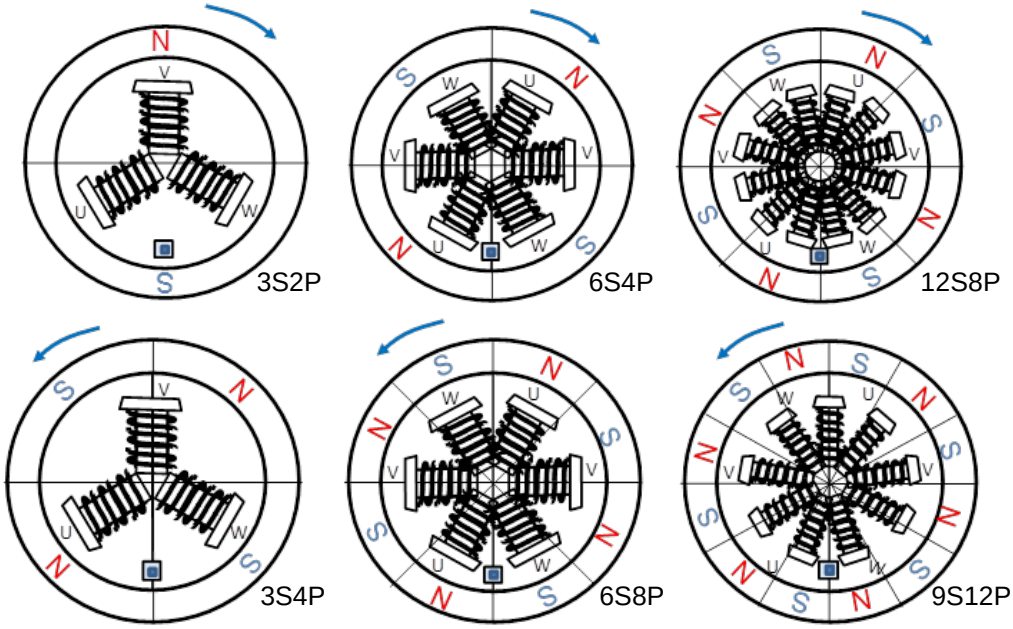


Figure 28. Schematic diagram of motor

Hall output polarity also needs to be set with the type of SP motors. It is shown in Figure 29, Figure 30

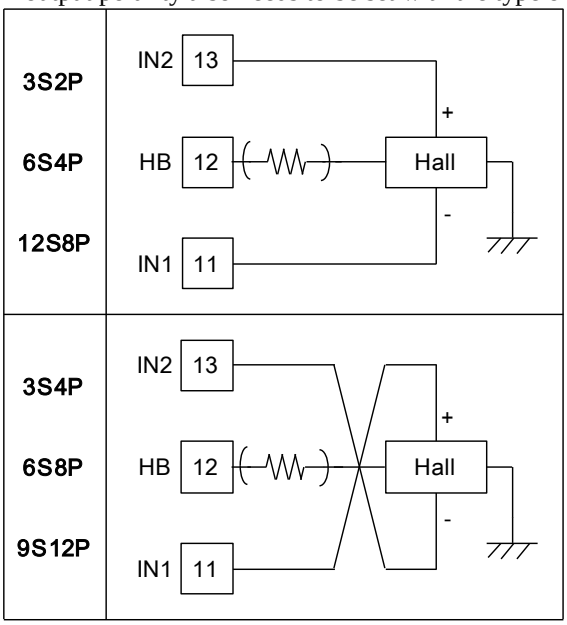


Figure 29. Hall element use connection

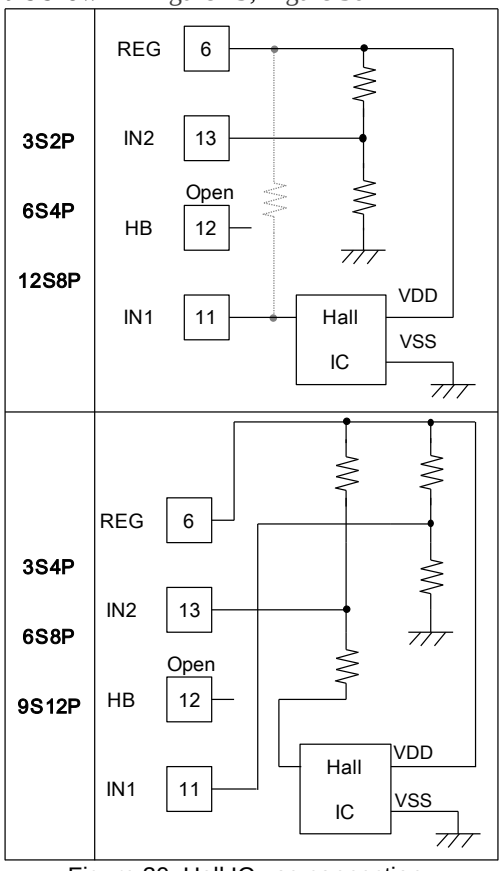


Figure 30. Hall IC use connection

DEVICE START-UP

The LV8811G, LV8813G will start driving, when the PWM signal is input at the PWMIN pin after a power supply is turned on.

COMMUTATION

The commutation timing is determined with respect to the one Hall sensor or Hall-IC signal, while conventional sensor-based BLDC motor drivers need three sensors.

OUTPUT WAVEFORM

The output PWM duty cycle is modulated so that the phase-to-phase voltage waveform is sinusoidal. Two phases are driven with PWM, while the other phase sunk to ground.

It can handle the rotational speed up to the 250Hz of FG frequency (electrical cycle). However, for high speed case, it depends on motor mechanical parameters. Low speed side recommends the rotational speed down to the 30Hz of FG frequency.

A wave pattern example is shown in Figure 31.

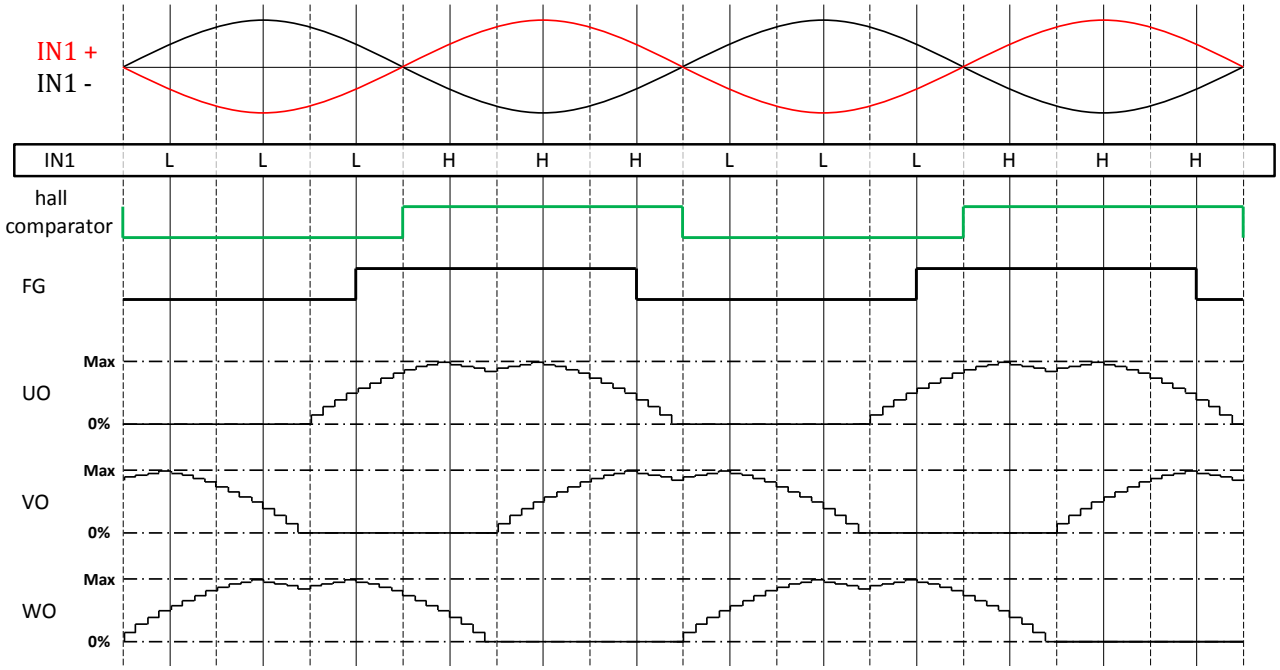


Figure 31. Timing chart example: Normal Rotation

The amplitude of current waveform is effected by input PWM duty cycle while the sinusoidal waveform is kept.

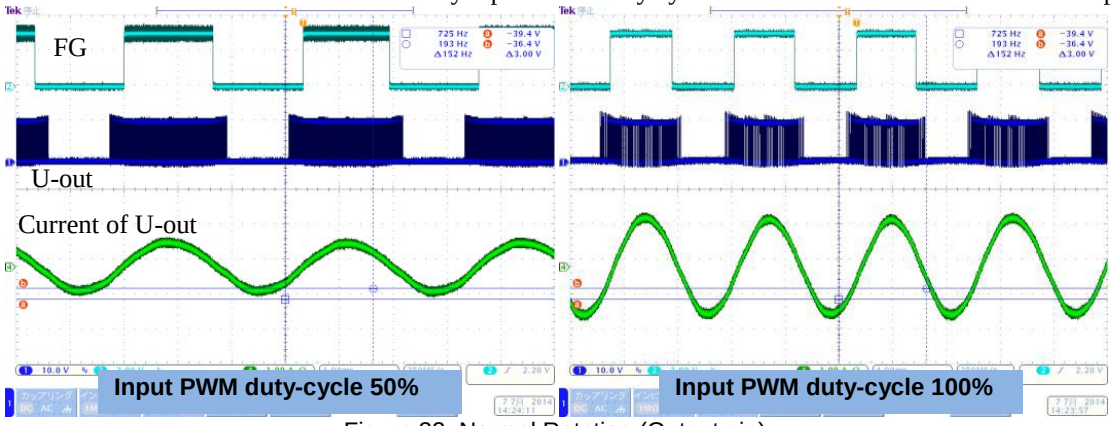


Figure 32. Normal Rotation (Output pin)

DETAIL OF THE ROTOR START POSITION ALIGNMENT

After detecting input PWM, the motor-rotor is aligned to the start position. The start position alignment is independent on the input PWM duty cycle, and applies the preset duty cycle described below.

[LV8811G] The output PWM duty cycle sequence for the rotor alignment consists of the three steps.

Alignment duty cycle 1st: 6%, 2nd: 5%, 3rd: 20%

[LV8813G] The output PWM duty cycle sequence for the rotor alignment consists of the single step.

Alignment duty cycle 50%

(Figure 33)

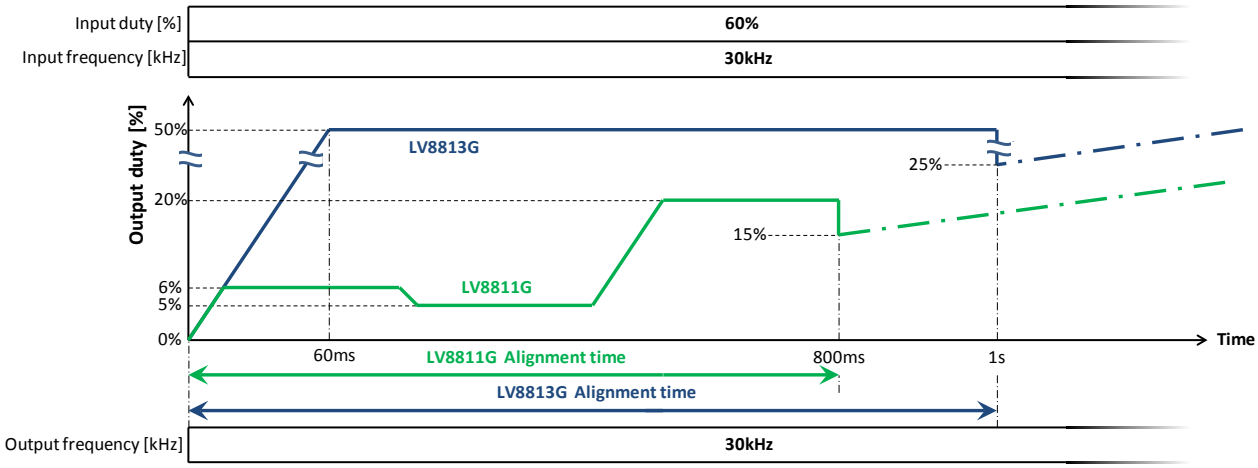


Figure 33. Timing chart example: Alignment duty cycle

ROTATION START-UP AND SOFT-START

After the adjustment of the start position, the output duty cycle begin from 15% (LV8811G) or 25% (LV8813G). the motor starts to rotate in sinusoidal drives, increasing output duty cycle (increment slope is 26[%/s]) till the output duty cycle reaches the target duty cycle. In case the input PWM duty cycle is under 20%, the output duty cycle decreases to the target duty cycle (decrement slope is 26[%/s]) after reaching 20%. After 32 FG pulses the lead angle increases to the target lead angle (tuned from PH1/PH2) by 1 degree steps at every FG edge. (Figure 34)

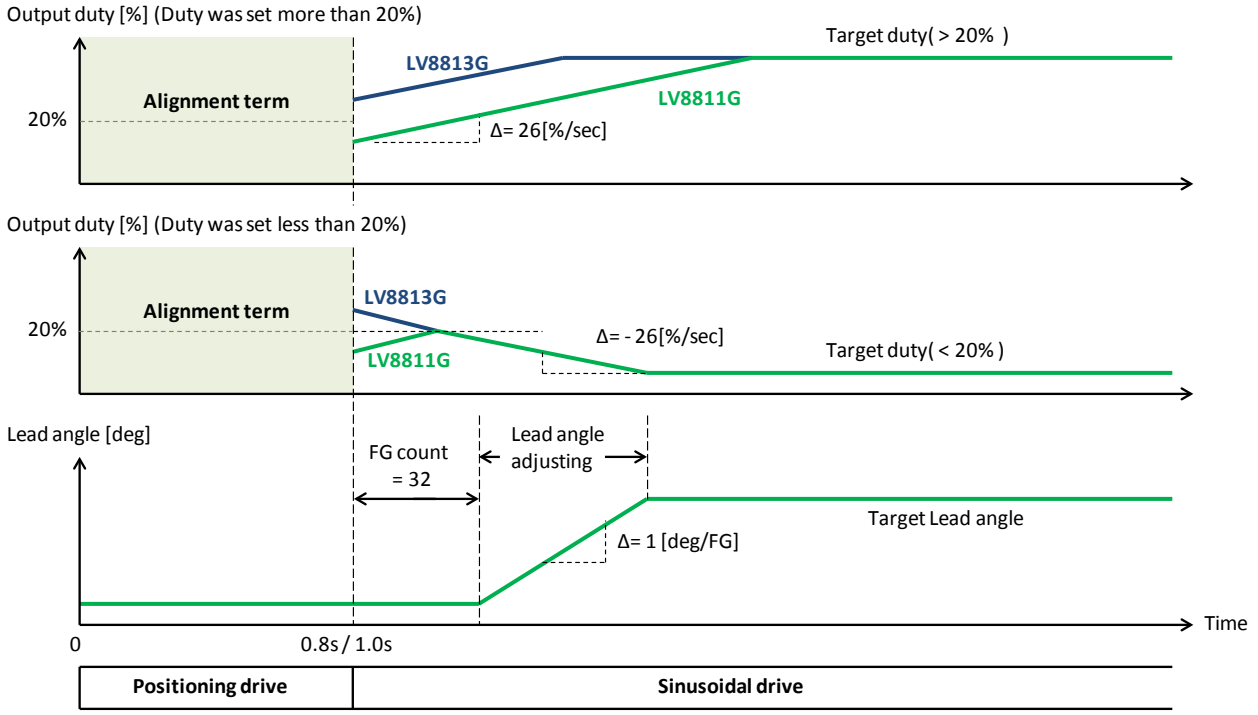


Figure 34. Timing chart example: Positioning and Soft start

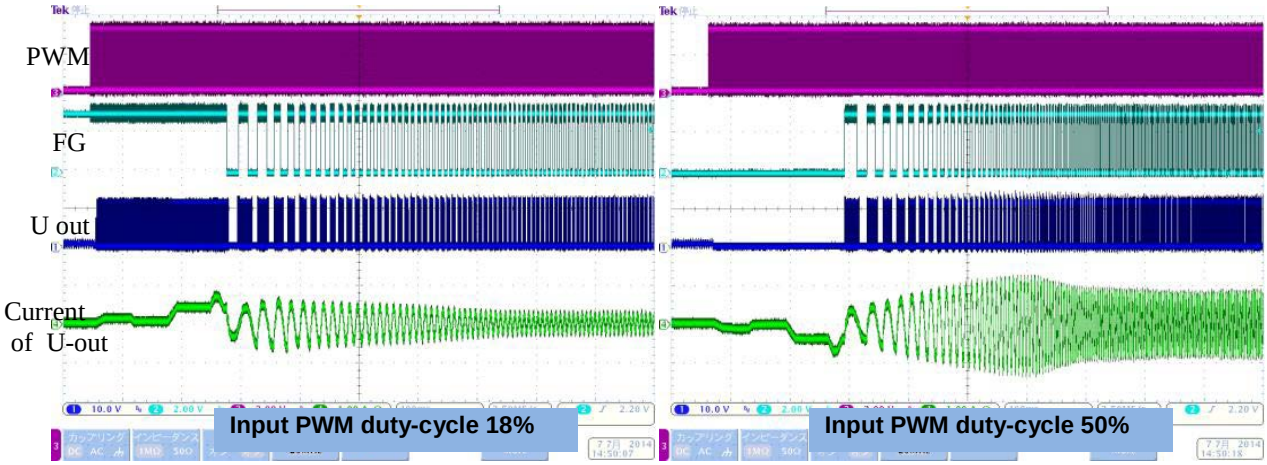


Figure 35. Alignment and Soft start (Case of the LV8811G)

DUTY CYCLE DECREASING AND STOP

When input PWM duty cycle is changed from high to low, the output duty cycle decreases gradually to low with the decrement slope of 26[%/s]. The target duty cycle is always updated at positive edge of FG. (Figure 36)

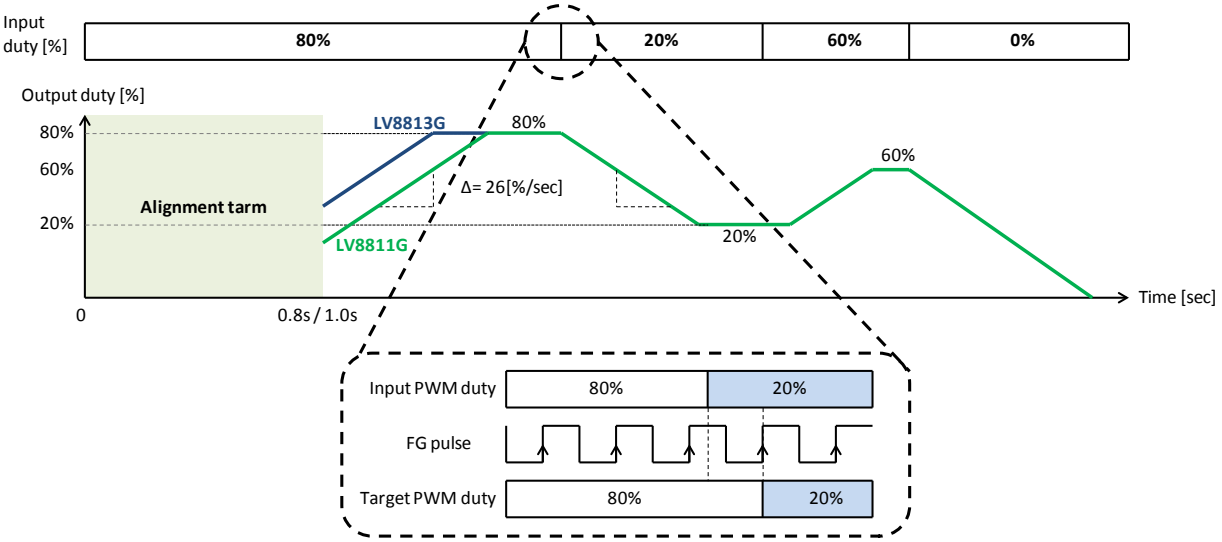


Figure 36. Timing chart example: When PWM Duty cycle changed (80% -> 20% -> 60% -> 0%)

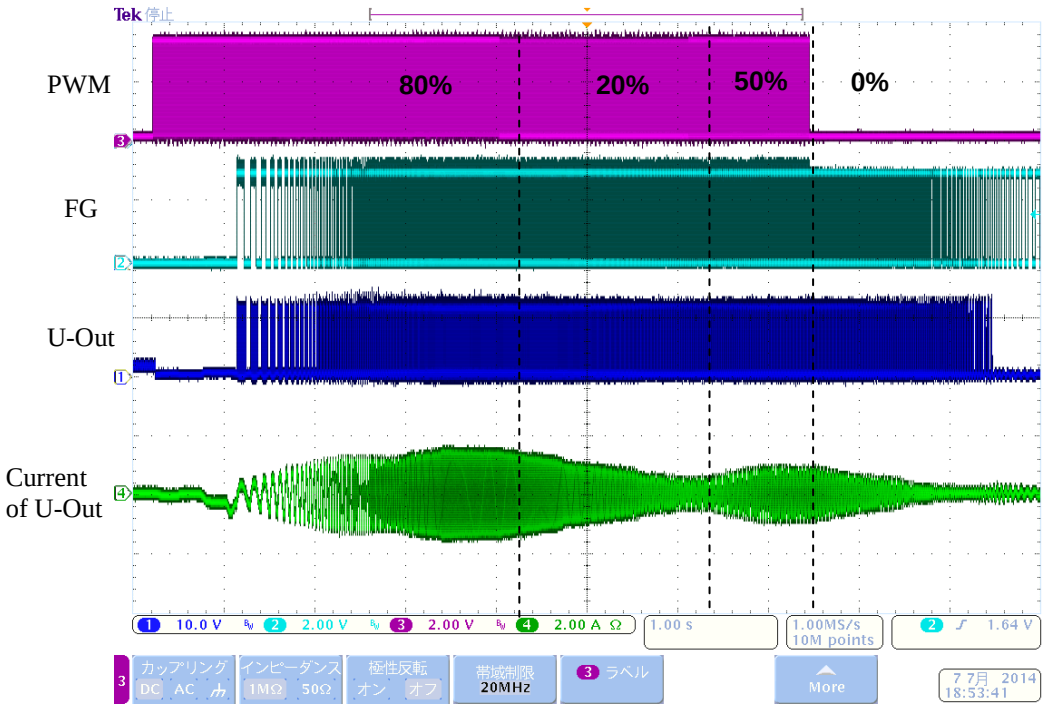


Figure 37. Input duty cycle changing (Case of the LV8811G)

OUTPUT FREQUENCY

When input PWM duty cycle is 100%, the output frequency is 66kHz generated from the internal oscillator. When input PWM duty cycle is changed from 100% to low (e.g. 50% with 30kHz), output frequency is changed from 66kHz to input PWM frequency (this case is 30kHz). When input PWM duty cycle is changed to 100% again, output frequency will remain last input frequency (this case is 30kHz). (Figure 38)

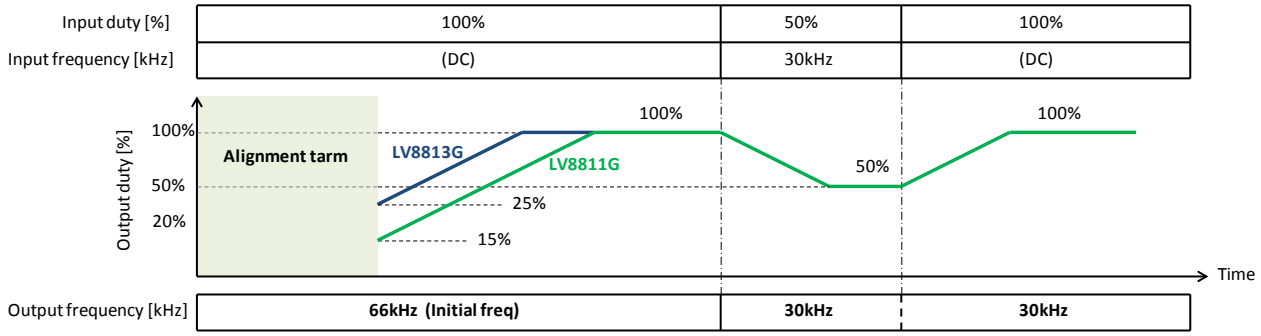


Figure 38. Timing chart example: Output frequency changing

PROTECTIONS

When THP (Thermal Protection) or CLM (Current Limiter) is detected, the output duty cycle decreases to the minimum duty cycle rapidly. After exiting the protection mode, the output duty cycle increases with 26[%/s] slope. When OVP(Over Voltage Protection) or LVD(Low Voltage Detection) signal is detected, all outputs are turned off. After OVP and LVD are released, outputs are turned on. (Figure 39)

When the current limiter is detected, the output duty cycle may be restricted before achieving target duty cycle. The output duty cycle decreases immediately by the current limiter. The current limiter is release, because the output duty cycle decreases. Herewith, the output duty cycle increases to the target duty cycle. And the current limiter is detected again, and the output duty cycle decreases. On/off of the current limiter is repeated, and the output duty cycle is limited. When the PWM input changes to low duty cycle that release CLM, the output duty cycle decreases gradually with normal slope rate of 26[%/s]. (Figure 40)

When current limiter activates with 100% input duty cycle, the output duty cycle is restricted before achieving target duty cycle (100%). When the PWM input changes from less than low duty cycle, the output duty cycle decreases to the input duty cycle immediately without slope rate. (Figure 41)

The level of current limiter is adjustable using the value of RF resistor.

The value of RF resistor should be set higher than the current drawn at 100% input duty cycle.

Lock detection and Lock protection

[LV8811G] It takes 5.68s for Lock protection time. Lock start time is 1.12s. This equals to the total of lock detect time and the alignment time. The protection-start time ratio is approx. 1:5. Output under lock protection is in Hi-Z state. (Figure 43)

[LV8813G] The lock protection behavior is same as LV8811G. However, the release time and restart time are changed as follows:

Lock protection time: 5.23s Lock start time: 1.76s

Protection-start ratio: approx. 1:3 (Figure 44)

When the lock start time, heat is generated that because IC turned on electricity to the motor. On the other, when the lock protection time, radiated heat that because IC turned off electricity to the motor.

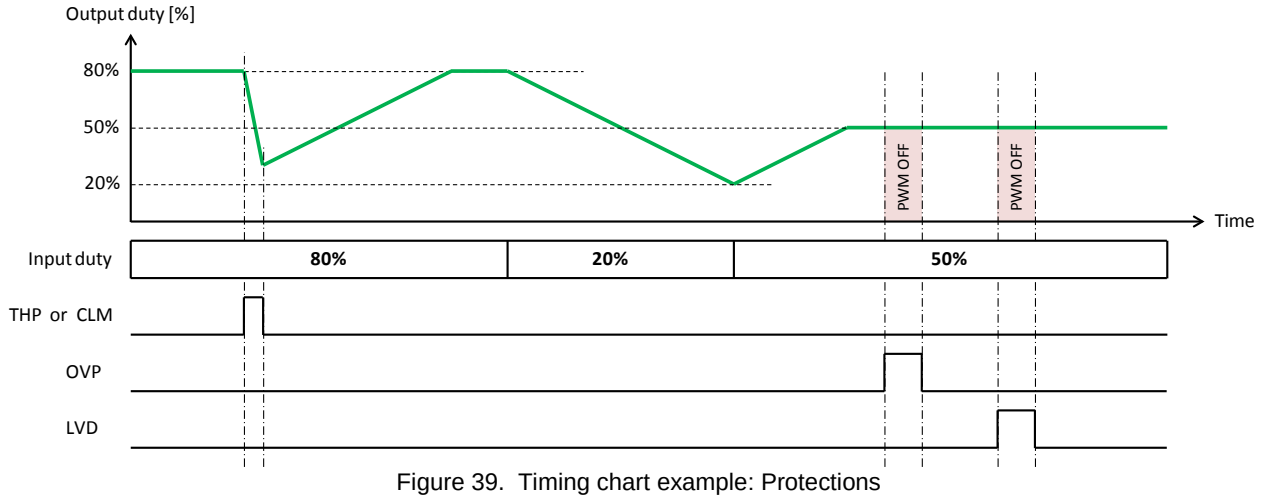


Figure 39. Timing chart example: Protections

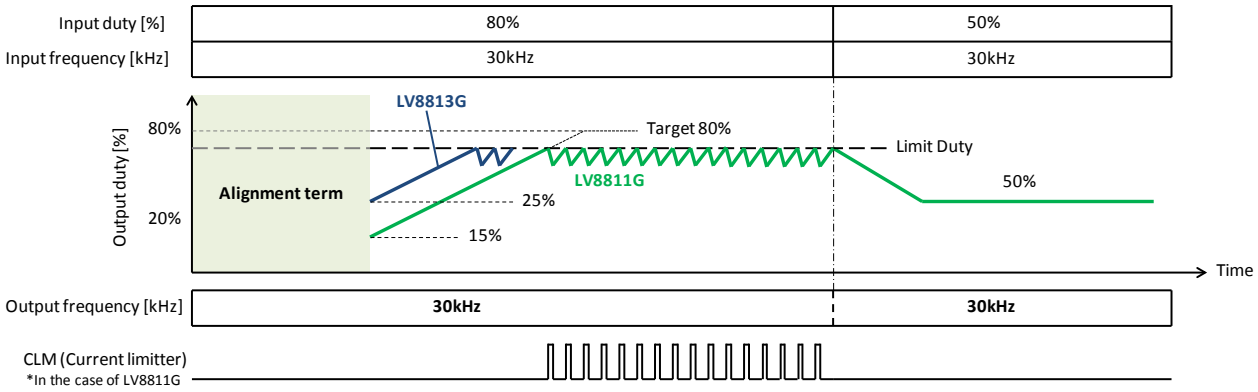


Figure 40. Timing chart example: Normal current limiter (e.g. input duty cycle 80% -> 50%)

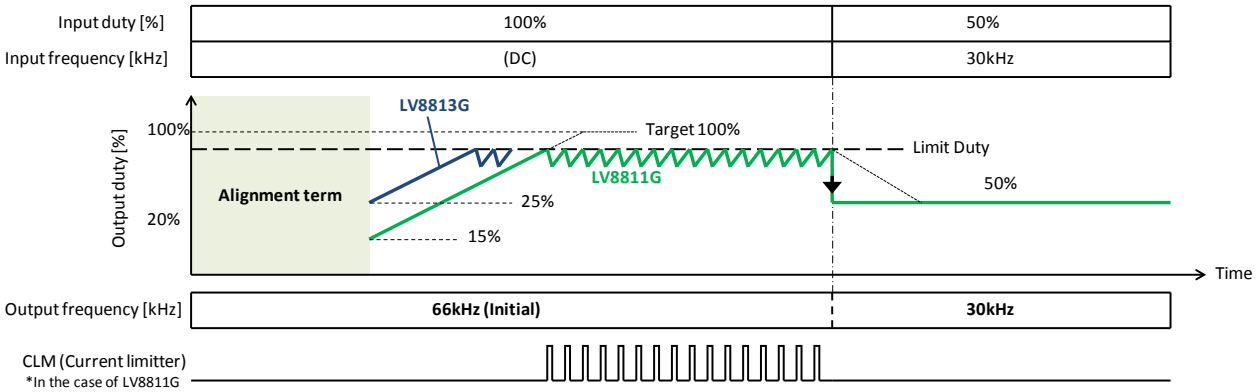


Figure 41. Timing chart example: Current limiter at input duty cycle 100%

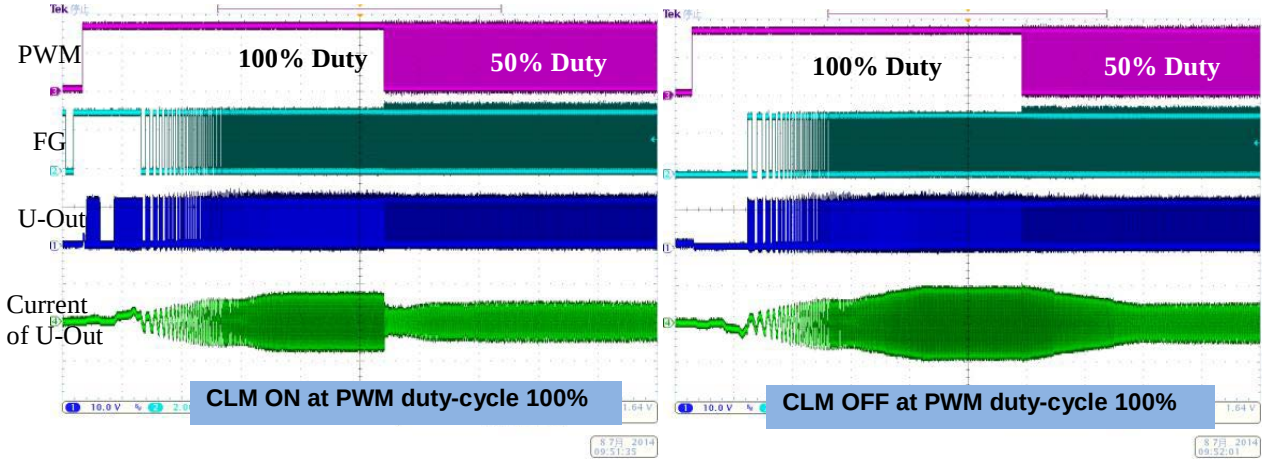
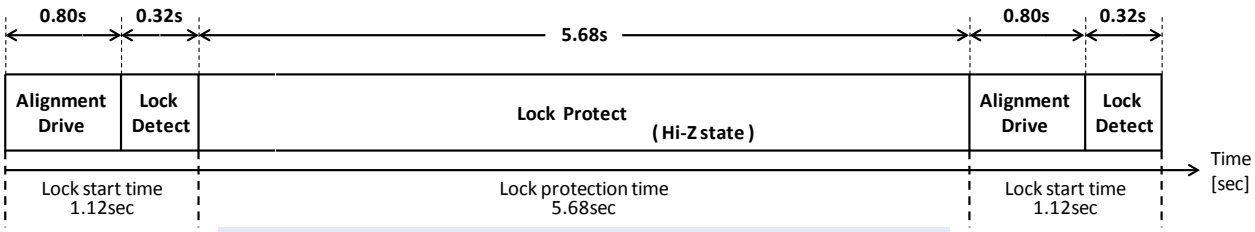
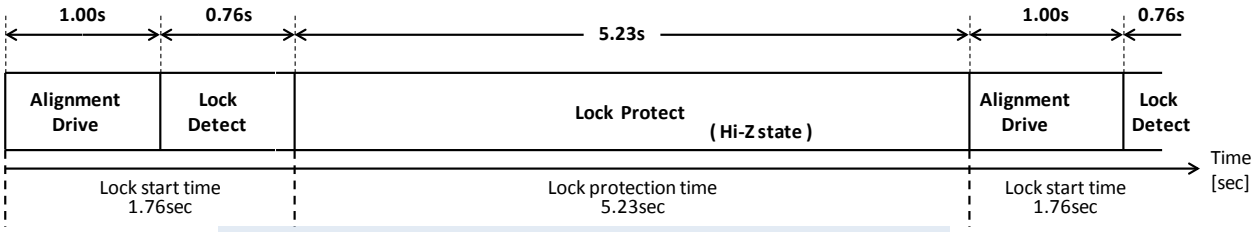


Figure 42. Inputting 100% with and without CLM (Case of the LV8811G)



Lock start time : Lock protection time = 1.12 : 5.68 ≈ **1: 5 (Protection-start ratio)**

Figure 43. Timing chart example: Lock Protection for LV8811G



Lock start time : Lock protection time = 1.76 : 5.23 ≈ **1: 3 (Protection-start ratio)**

Figure 44. Timing chart example: Lock Protection for LV8813G

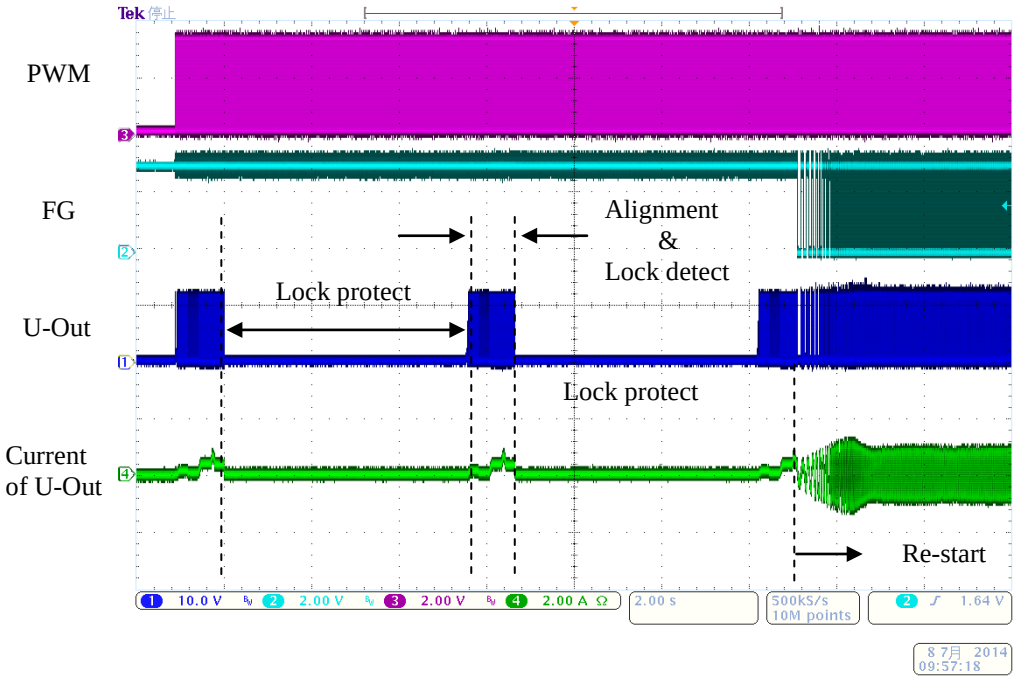


Figure 45. Lock Protection (Case of the LV8811G)

PWM DUTY CYCLE CONTROL BY ANALOG VOLTAGE

The duty cycle of PWM output is determined by comparison of CPWM oscillation and DC level which is input to VTH pin. When CPWM level is lower than VTH, the PWM output applies the voltage to the coil from the power supply. When CPWM level is higher than VTH, the PWM output is switched to the current circulation state with self-induction of the coil.

The DC level of VTH can control between V_{REG}×18% and V_{REG}×67%. But the PWM pulse width must not make less than 200ns. The pulse width of 0s is accepted. (Figure 46)

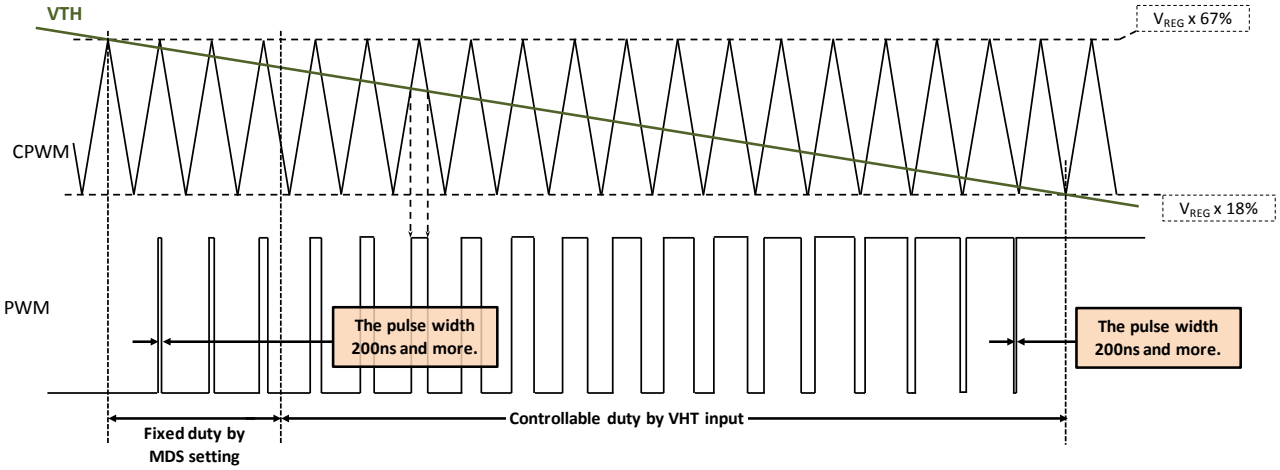


Figure 46. PWM Duty cycle control by CPWM and the VTH voltage

The relations of V_{VTH} and output PWM duty cycle are clculated by following equation.

$$V_{VTH} = V_{CPWMH} - (V_{CPWMH} - V_{CPWML}) \times \frac{D_{OUT}}{100}$$

Where

D_{OUT} = Output PWM duty cycle

For example, when the output PWM duty cycle is set in 30%, it can be determined by follows.

$$V_{VTH} = 2.01[V] - (2.01[V] - 0.54[V]) \times \frac{30[\%]}{100}$$
$$= 1.569[V]$$

When the output PWM duty cycle is set in 100%, it is recommended to set the VTH input level lower than V_{CPWML}. In addition, when the output PWM duty cycle is set in 0%, it is recommended to set the VTH input level higher than V_{CPWMH}.

The input range of VTH is calculated in the following equation. (Figure 47)

$$h' = \frac{t'}{t} \times h$$

$$\text{VTH control range}[V] = 0.18V_{REG} + h' \sim 0.67V_{REG} - h'$$

Where,

$$h = V_{CPWMH}[V] - V_{CPWML}[V]$$

$$t = \frac{(V_{CPWMH} - V_{CPWML})[V] \times C_5[pF]}{I_{CPWMSI/O}[A]}$$

$$t' = 200ns \div 2 = 100ns$$

*C_5 is the CPWM pin external capacity. Refer to page.5 and 17

For example, when 330[pF] is used for CPWM capacity, can be determined by followings

$$h' = \frac{0.1[us]}{16.73[us]} \times 1.47[V] = 8.79[mV]$$

From the above-mentioned result, the range of the VTH input voltage is

·Full speed
$0.18V_{REG}$ or less than,
· Rotational speed control
$0.18V_{REG}$+8.79[mV] to $0.67V_{REG}$-8.79[mV],
· Motor stop
$0.67V_{REG}$ or more than

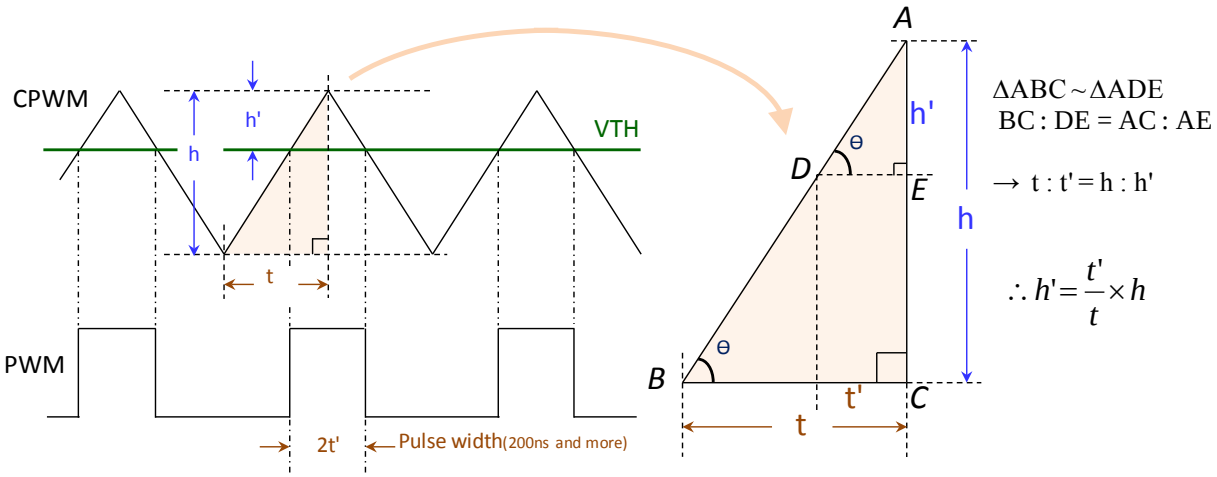


Figure 47. Reference of the calculation of the VTH input range

PARAMETER SETTING BY CONSTANT VOLTAGE

PH1, PH2 and MDS can be set by the external DC voltage levels. PH1 and PH2 are used for setting the lead angle. MDS is for setting minimum duty cycle. The input span of these pins is 0 to 3V (V_{REG}). The full scale is divided by 64 steps, thus the resolution is 47mV/step. Excluding the lowest 3 steps and the highest 2 steps, the DC voltage is translated to the parameters linearly. Hence, the linear setting range is 0.141V to 2.906V. The voltage within the lowest 3 steps (0 to 0.141V) selects the default value. As for the highest 2 steps is below.

MDS

- Lowest 3 steps is FG cycle 1 electrical, and default setting for MDS.
- Highest 2 steps is FG cycle 2 electrical, and default setting for MDS.

PH1/PH2

- Highest 2 steps is prohibit.

(Figure 48)

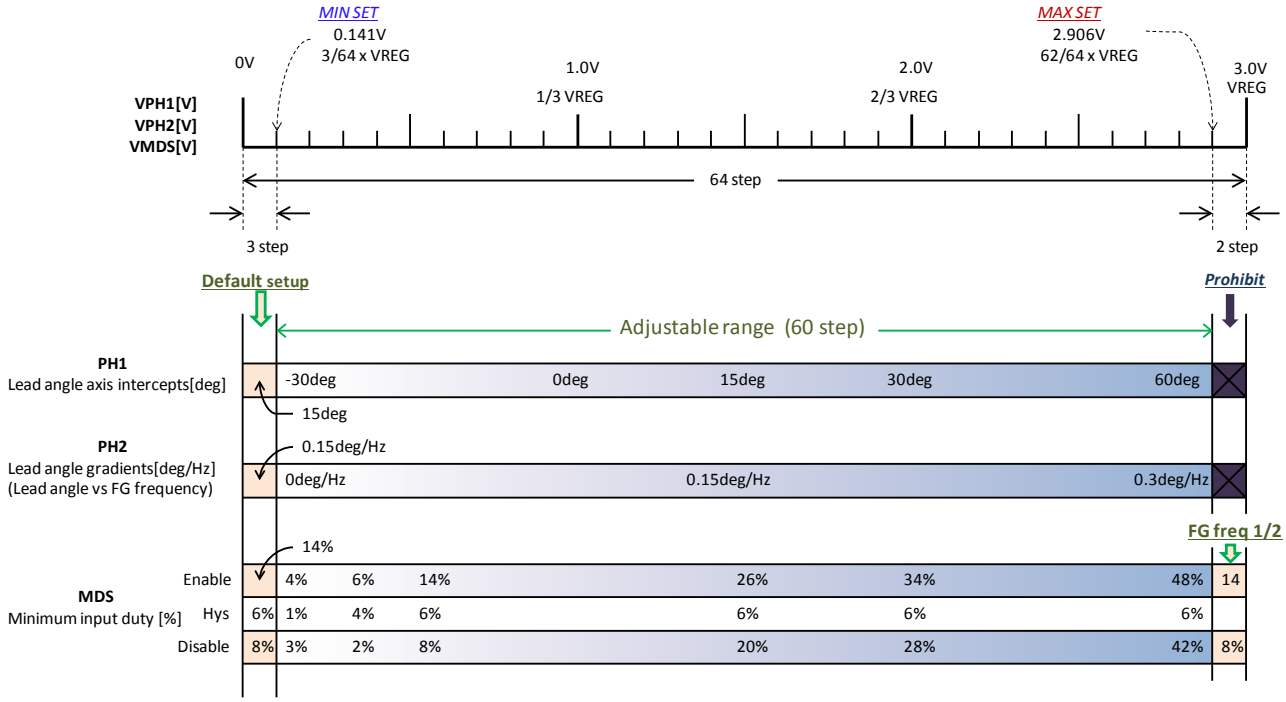


Figure 48. Pin-set PH1, PH2 and MDS

SETTING MINIMUM PWM DUTY CYCLE

When the input PWM duty cycle is less than the minimum duty cycle, which is set by MDS pin voltage, the output duty cycle becomes 0%. And, this threshold has hysteresis. In the meantime, MDS pin is also used for the FG frequency setting. (Figure 49, Figure 50)

V_{MDS} range [V]	0~0.141	0.141~ 0.282	0.282~ 0.752	0.752~ 2.906	2.906 ~ 3.0
Minimum input duty cycle hysteresis [%]	6	1	4	6	6
Minimum input duty cycle for enable [%]	14	$15.9V_{MDS} + 1.763$			14
Minimum input duty cycle for disable [%]	8	$15.9V_{MDS} + 1.763 - hys$			8
FG cycle	1 electrical				2 electrical

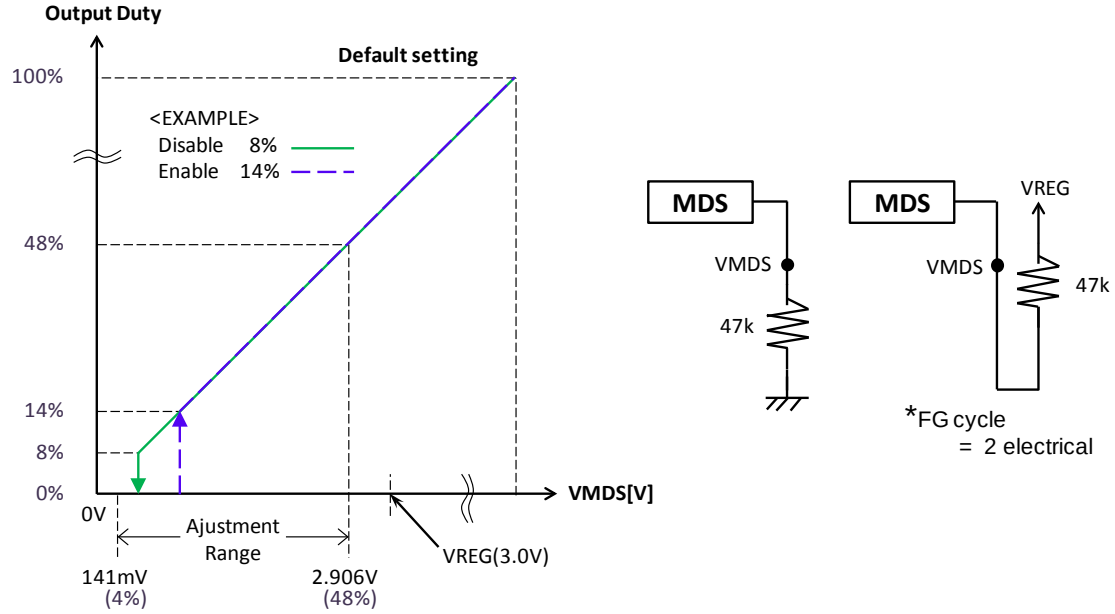


Figure 49. Example Setting Minimum PWM duty cycle (case of default setting)

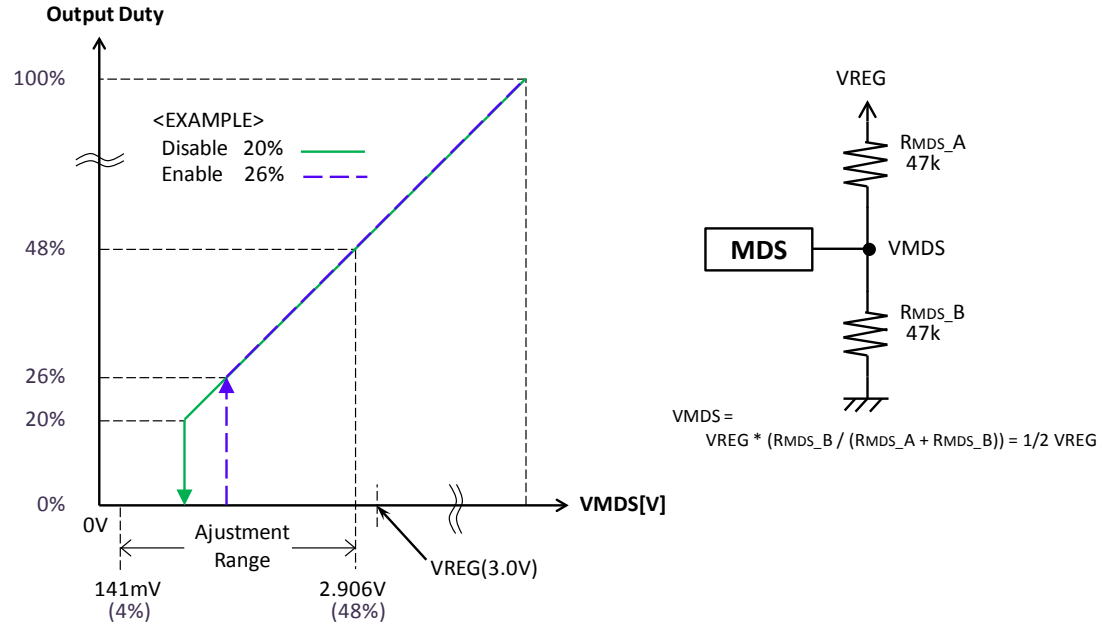


Figure 50. Example Setting Minimum PWM duty cycle (case of 1/2 V_{REG} setting)

SETTING LEAD ANGLE

PH1 and PH2 pin determine the optimum lead angle for a specific speed range. PH1 provides lead angle at the low speed, The PH2 pin provides lead angle slant for speed (FG frequency). Both pins become the initial value in GND. (Figure 51, Figure 52, Figure 53)

The lead angle P (typ.) is determined by the following equation.

$$P = Af_{FG} + B$$
$$A = 0.1081V_{PH2} - 0.015$$
$$B = 32.54V_{PH1} - 34.58$$

where f_{FG} is FG frequency [Hz]

when V_{PH1} and $V_{PH2} = 0$

$$A = 0.15[\text{deg/Hz}]$$
$$B = 15[\text{deg}]$$

Note: The equations above are based on the ideal case as a reference for the user application design. It must be readjusted by an experimental confirmation with the actual movement and the motor to be used.

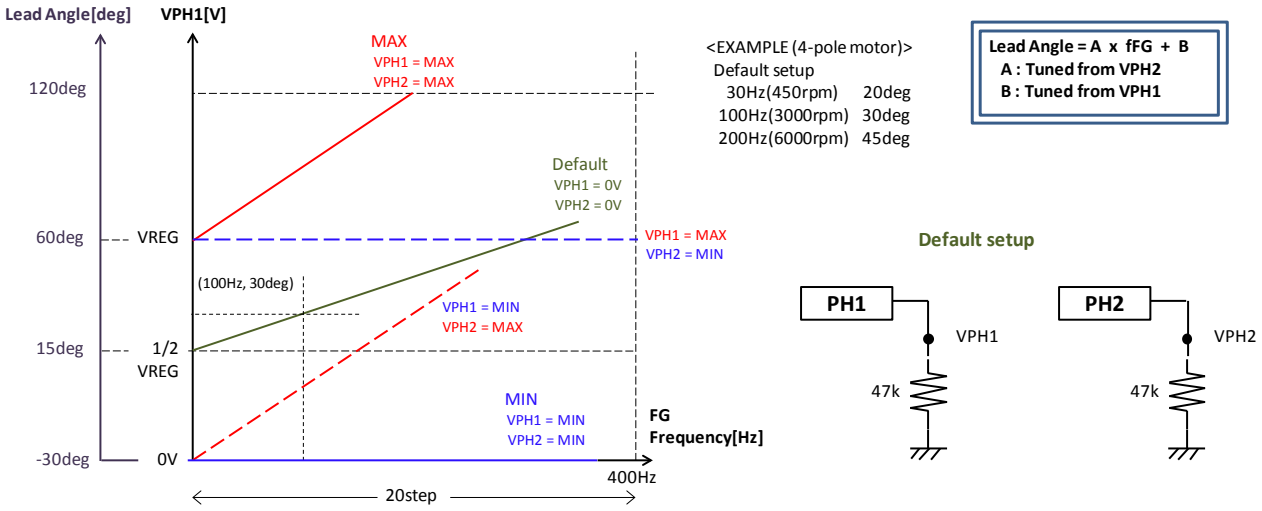


Figure 51. Example Setting Lead Angle (case of default setting)

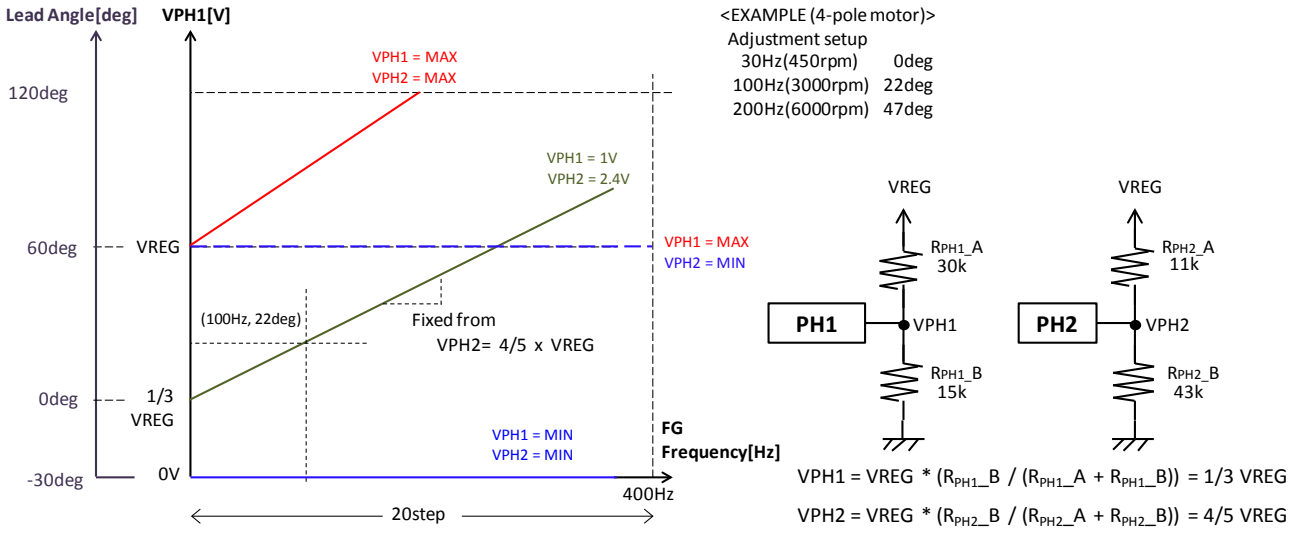


Figure 52. Example Setting Lead Angle (case of 1/3V_{REG} and 4/5V_{REG} setting)

Sinusoidal PWM signals are generated from 1-hall signal, handling the lead angle parameters.

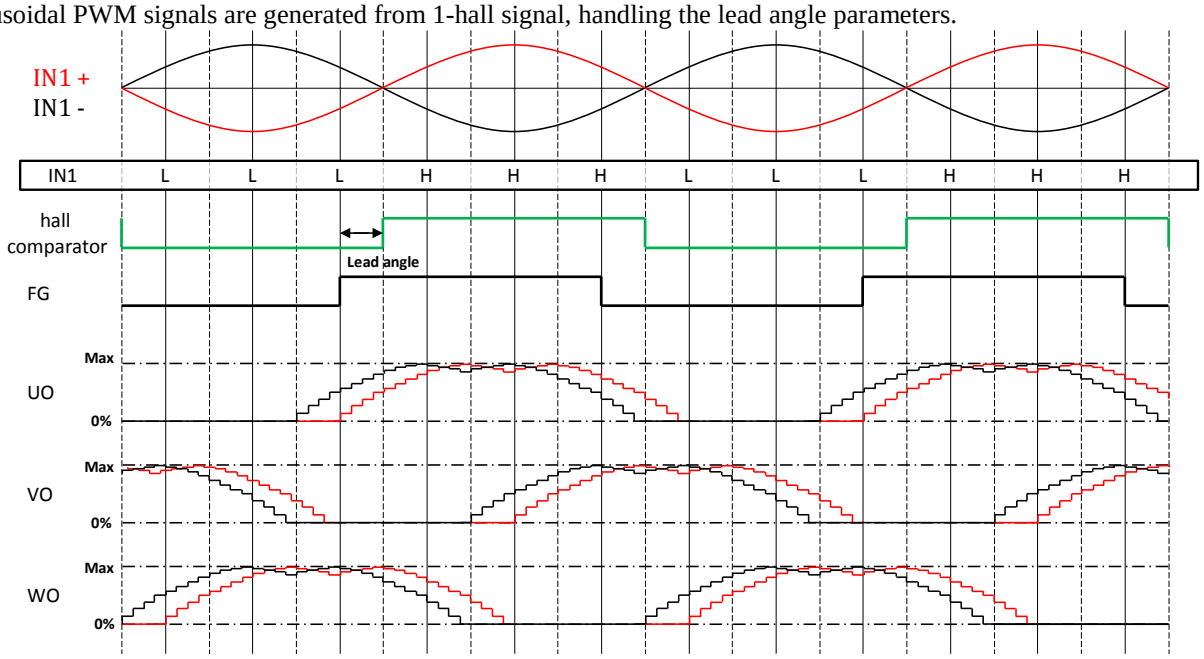


Figure 53. Timing chart example: Lead Angle

Efficiency and sinusoidal waveform can be optimized by changing the voltage levels of PH1 and PH2. First, adjust PH1 in low speed (low PWM duty cycle) such as 20%. In the examples below, VPH1 = ~1.5V is the best case for efficiency and the shape of sinusoidal wave. After optimizing VPH1, adjust VPH2 adjusted in high speed (high PWM duty cycle) such as 100%. (Figure 54)

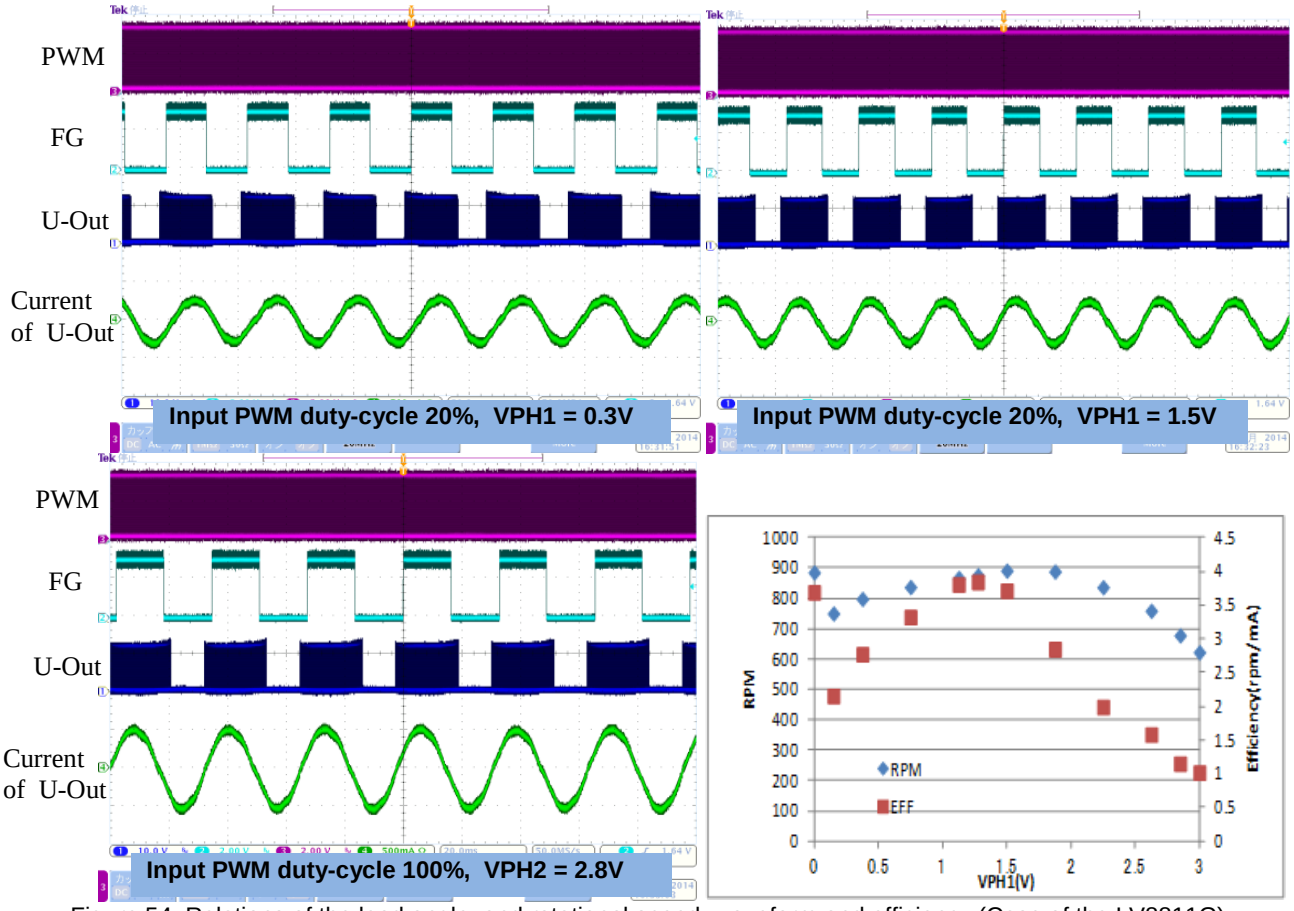


Figure 54. Relations of the lead angle and rotational speed, waveform and efficiency (Case of the LV8811G)

PCB GUIDELINES

VCC AND GROUND ROUTING

Make sure to short-circuit VCC line externally by a low impedance route on one side of PCB. As high current flows into PGND, connect it to GND through a low impedance route.
The capacitance connected between the VCC pin and the opposite ground is to stabilize the battery. Make sure to connect an electrolytic capacitor with capacitance value of about 10uF (3.3uF or greater) to eliminate low frequency noise. Also, to eliminate high frequency noise, connect a capacitor of superior frequency characteristics, with capacitance value of about 0.1uF and make sure that the capacitor is connected as close to the pin as possible. Allow enough room in the design so the impact of PWM drive and kick-back does not affect other components. Especially, when the coil inductance is large and/or the coil resistance is small, current ripple will rise so it is necessary to use a high-capacity capacitor with superior frequency characteristics. Please note that if the battery voltage rises due to the impact of the coil kick-back as a result of the use of diode for preventing the break down caused by reverse connection, it is necessary to either increase the capacitance value or place Zener diode between the battery and the ground so that the voltage does not exceed absolute maximum voltage.
When the electrolytic capacitor cannot be used, add the resistor with the value of about 1Ω (R20) and a ceramic capacitor with the capacitor value of about 10μF (C20) in series for the alternative use. When the battery line is extended, (20-30 cm to 2-3 m), the battery voltage may overshoot when the power is supplied due to the impact of the routing of the inductance. Make sure that the voltage does not exceed the absolute maximum standard voltage when the power supply turns on.
These capacitance values are just for reference, so the confirmation with the actual application is essential to determine the values appropriately.

EXPOSED PAD

The exposed pad is connected to the frame of the LV8811G, LV8813G. Therefore, do not connect it to anywhere else other than ground. If GND and PGND are in the same plane, connect the exposed pad to the ground plane. Else, if GND and PGND are separated, connect the exposed pad to GND.

RF ROUTING

Power current (output current) flows through the RF line. Make sure to short-circuit the line from VCC through RF as well as VCC. The RF resistance must choose the enough power rating.

NC PIN UTILIZATION

NC pins are not connected internally inside the LV8811G, LV8813G. If the NC pin has to be connected to another pin for the development of the PCB board, make sure to assign the pin using wires of stable voltage and current with lower impedance value.

MOTOR DRIVER OUTPUT PINS

Since the pins have to tolerate surge of current, make sure that the wires are thick and short enough when designing the PCB board.

THERMAL TEST CONDITIONS

Size: 57.0mm × 57.0mm × 1.6mm (Double layer PCB)
Material: Glass epoxy
Copper wiring density: L1 = 80% / L2 = 85%

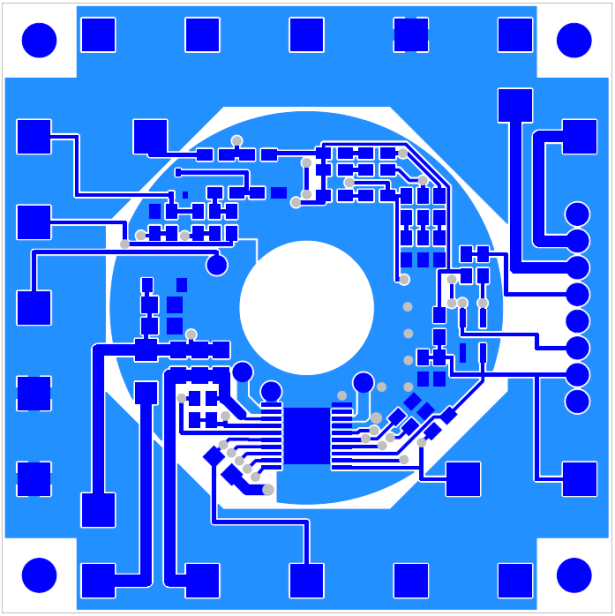
RECOMMENDATION

The thermal data provided is for the thermal test condition where 95% or more of the exposed die pad is soldered.
It is recommended to derate critical rating parameters for a safe design. Electrical parameters that are recommended to be derated are operating voltage, operating current, junction temperature, and device power dissipation. The recommended derating for a safe design is as shown below:

Maximum 80% or less for operating voltage
Maximum 80% or less for operating current
Maximum 80% or less for junction temperature

Check solder joints and verify reliability of solder joints for critical areas such as exposed die pad, power pins and grounds.
Any void or deterioration, if observed, in solder joint of these critical areas parts, may cause deterioration in thermal conduction and that may lead to thermal destruction of the device.

L1 : Copper wiring pattern diagram (top)



L2 : Copper wiring pattern diagram (bottom)

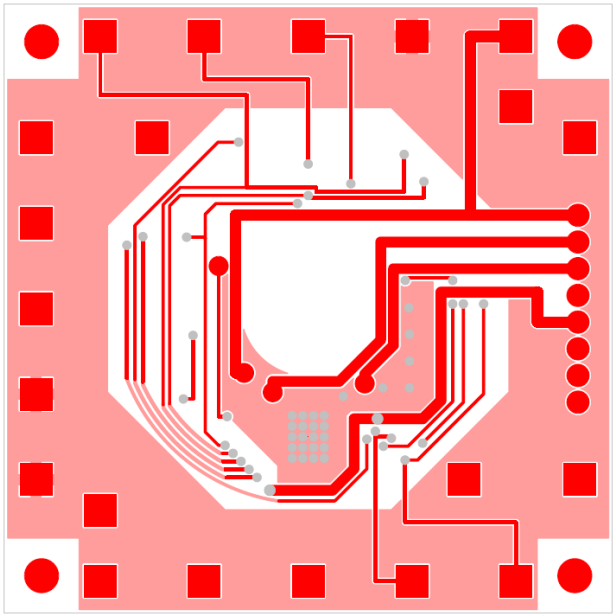
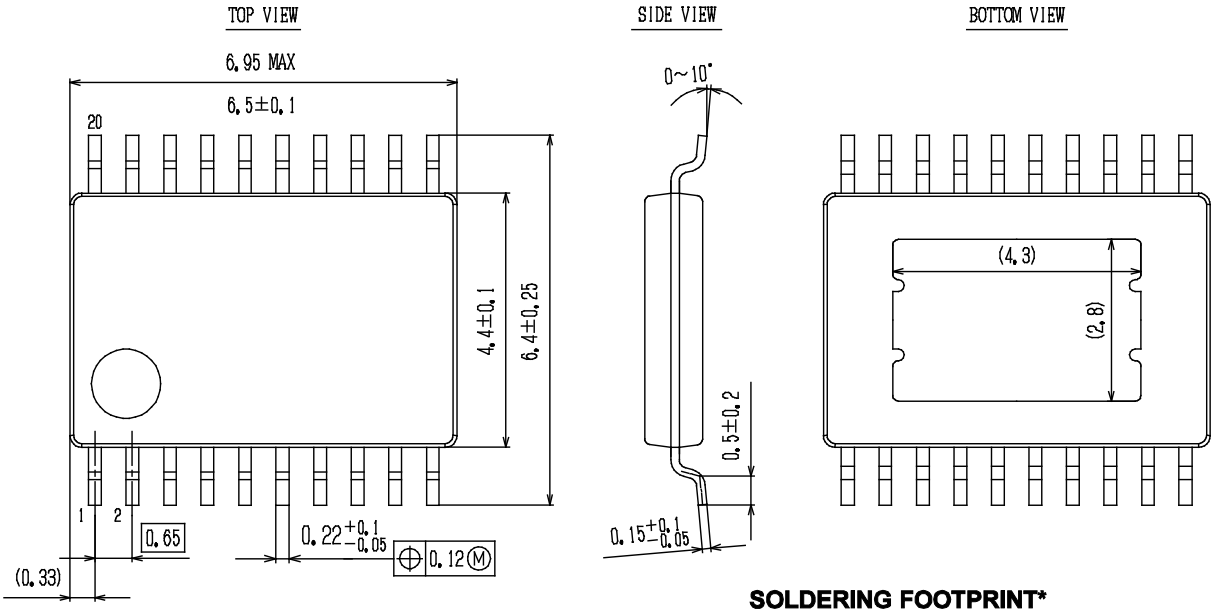
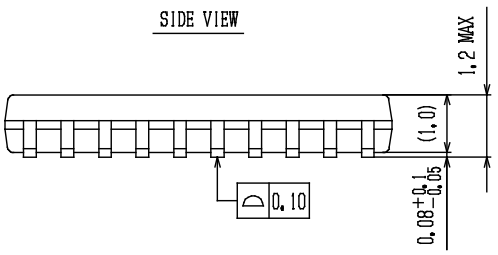


Figure 55. Pattern Diagram of Top and Bottom Layer

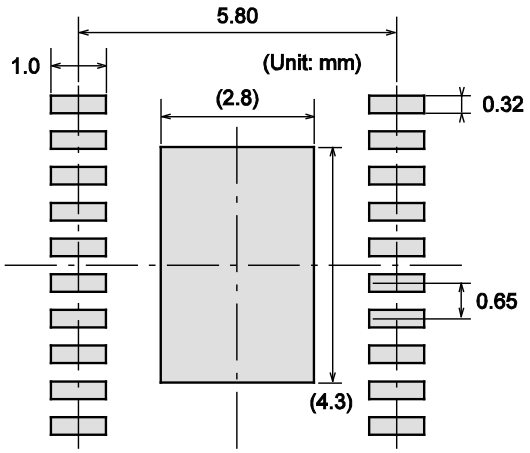
PACKAGE DIMENSIONS

TSSOP20 4.4x6.5 / TSSOP20J (225 mil)
CASE 948AZ
ISSUE A





SOLDERING FOOTPRINT*



NOTES: 1. The measurements are not to guarantee but for reference only.
2. Please take appropriate action to design the actual Exposed Die Pad and Fin portion.
3. After setting, verification on the product must be done.
(Although there are no recommended design for Exposed Die Pad and Fin portion Metal mask and shape for Through! Hole pitch (Pitch & Via etc), checking the soldered joint condition and reliability verification of soldered joint will be needed. Void • gradient • insufficient thickness of soldered joint or bond degradation could lead to IC destruction because thermal conduction to substrate becomes poor.)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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LV8813G-AH LV8811G-AH