ESD8451, SZESD8451

ESD Protection Diodes

Low Capacitance ESD Protection Diode for High Speed Data Line

The ESD8451 Series ESD protection diodes are designed to protect high speed data lines from ESD. Ultra−low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive high speed data lines.

Features

- Low Capacitance (0.30 pF Max, I/O to GND)
- Protection for the Following IEC Standards:
  IEC 61000−4−2 (Level 4)
  ISO10605 330 pF / 2 kΩ ±30 kV Contact
- Low ESD Clamping Voltage
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- USB 3.0
- MHL 2.0
- eSATA

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T_J	−55 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Seconds)	T_L	260	°C
IEC 61000−4−2 Contact (ESD) IEC 61000−4−2 Air (ESD)	ESD ESD	±15 ±15	kV kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

See Application Note AND8308/D for further description of survivability specs.

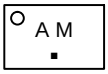
ON Semiconductor®

www.onsemi.com

MARKING DIAGRAMS

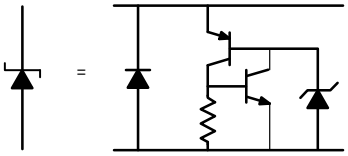
X3DFN2
CASE 152AF

XDFN2
CASE 711AM



P, A = Specific Device Code
M = Date Code

PIN CONFIGURATION AND SCHEMATIC



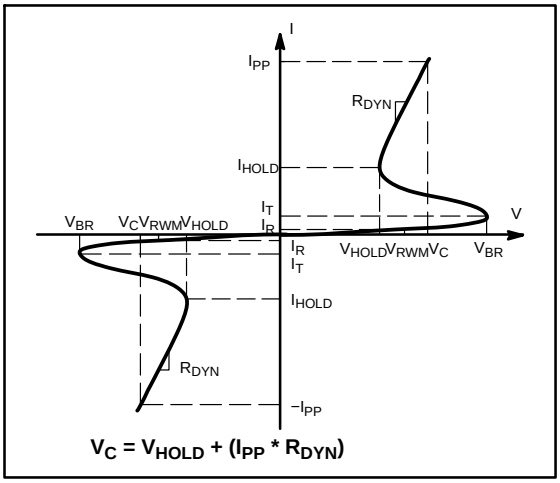
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
V_{RWM}	Working Peak Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
V_{HOLD}	Holding Reverse Voltage
I_{HOLD}	Holding Reverse Current
R_{DYN}	Dynamic Resistance
I_{PP}	Maximum Peak Pulse Current
V_C	Clamping Voltage @ I_{PP} $V_C = V_{HOLD} + (I_{PP} * R_{DYN})$



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	I/O Pin to GND			3.3	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, I/O Pin to GND	5.5	7.9	8.3	V
Reverse Leakage Current	I_R	V_{RWM} = 3.3 V, I/O Pin to GND			500	nA
Reverse Holding Voltage	V_{HOLD}	I/O Pin to GND		2.05		V
Holding Reverse Current	I_{HOLD}	I/O Pin to GND		17		mA
Clamping Voltage (Note 1)	V_C	IEC61000−4−2, ±8 KV Contact				V
ESD8451MUT5G Clamping Voltage	V_C	I_{PP} = 3.7 A, 8/20 μs pulse			13.7	V
ESD8451N2T5G Clamping Voltage	V_C	I_{PP} = 5.0 A, 8/20 μs pulse			17.0	V
ESD8451MUT5G Clamping Voltage TLP (Note 2)	V_C	I_{PP} = 8 A } IEC 61000−4−2 Level 2 equivalent (±4 kV Contact, ±4 kV Air)		11.0		V
		I_{PP} = 16 A } IEC 61000−4−2 Level 4 equivalent (±8 kV Contact, ±8 kV Air)		19.0		
ESD8451N2T5G Clamping Voltage TLP (Note 2)	V_C	I_{PP} = 8 A } IEC 61000−4−2 Level 2 equivalent (±4 kV Contact, ±4 kV Air)		9.0		V
		I_{PP} = 16 A } IEC 61000−4−2 Level 4 equivalent (±8 kV Contact, ±8 kV Air)		16.0		
ESD8451MUT5G Dynamic Resistance	R_{DYN}	Pin1 to Pin2 Pin2 to Pin1		1.0 1.0		Ω
ESD8451N2T5G Dynamic Resistance	R_{DYN}	Pin1 to Pin2 Pin2 to Pin1		0.84 0.84		Ω
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz		0.20	0.30	pF
Junction Capacitance	C_J	V_R = 0 V, f = 2.5 GHz		0.19	0.25	pF

1. For test procedure see Figure 16 and application note AND8307/D.
2. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.
   TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 4 ns, averaging window; t_1 = 30 ns to t_2 = 60 ns.

TYPICAL CHARACTERISTICS

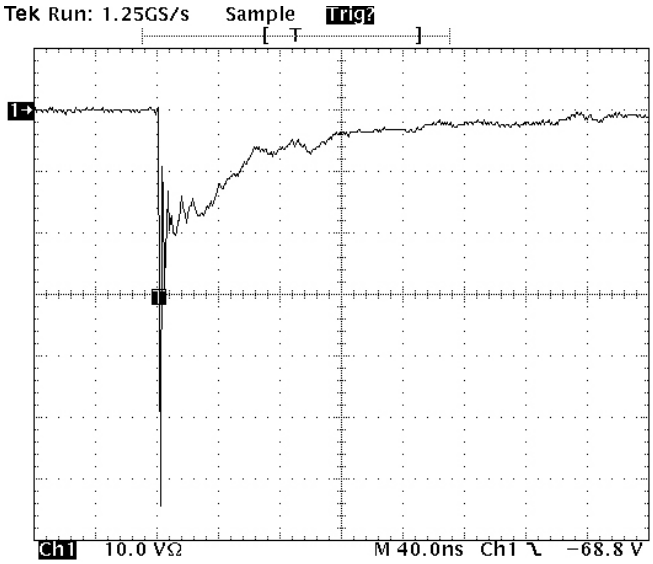


Figure 1. ESD8451N2 ESD Clamping Voltage Screenshot Negative 8kV Contact per IEC61000−4−2

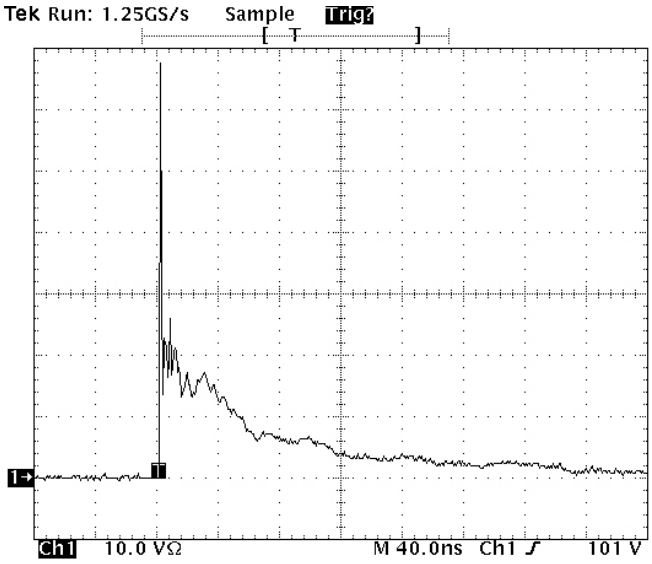


Figure 2. ESD8451N2 ESD Clamping Voltage Screenshot Positive 8kV Contact per IEC61000−4−2

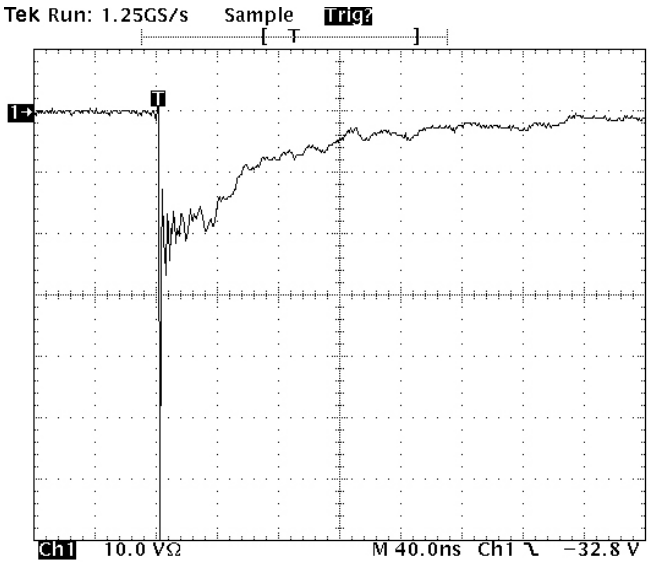


Figure 3. ESD8451MU ESD Clamping Voltage Screenshot Negative 8kV Contact per IEC61000−4−2

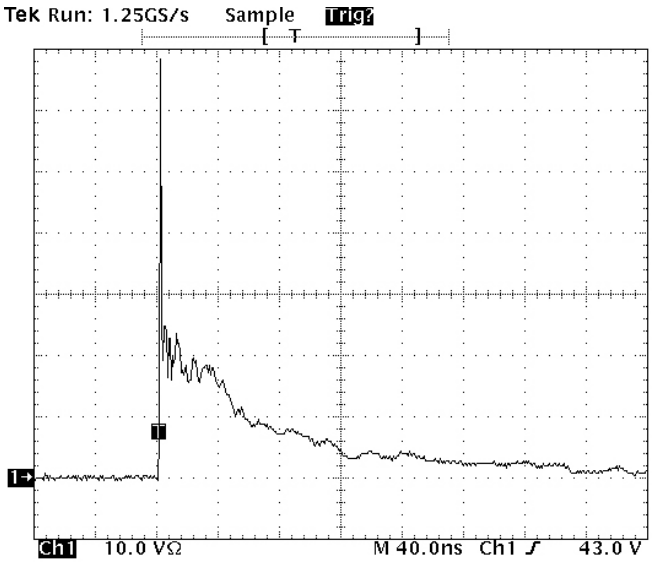


Figure 4. ESD8451MU ESD Clamping Voltage Screenshot Positive 8kV Contact per IEC61000−4−2

TYPICAL CHARACTERISTICS

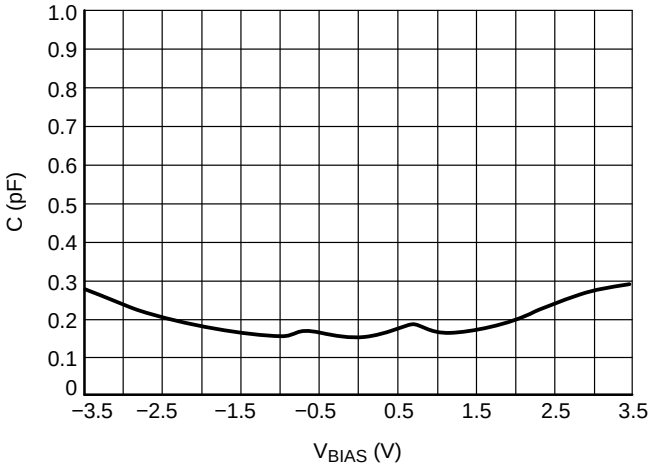


Figure 5. ESD8451MUT5G CV Characteristics

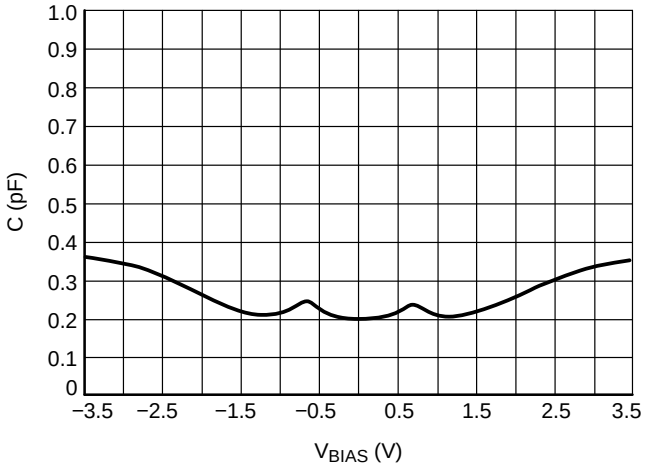


Figure 6. ESD8451N2T5G CV Characteristics

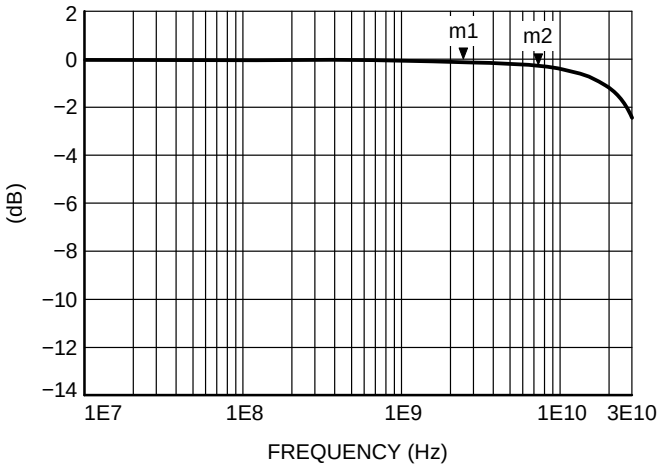


Figure 7. ESD8451MUT5G S21 Insertion Loss

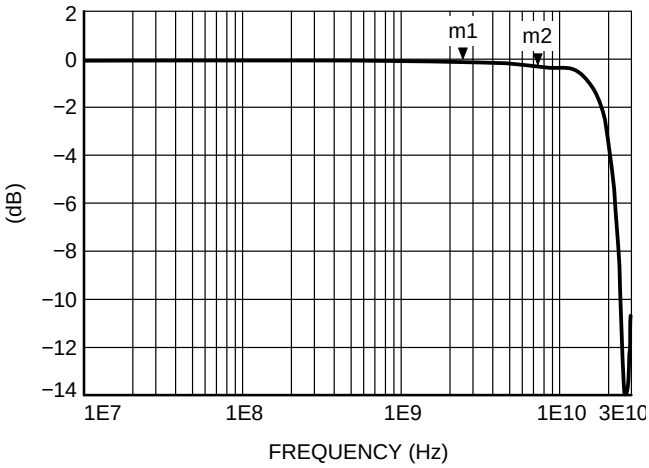


Figure 8. ESD8451N2T5G S21 Insertion Loss

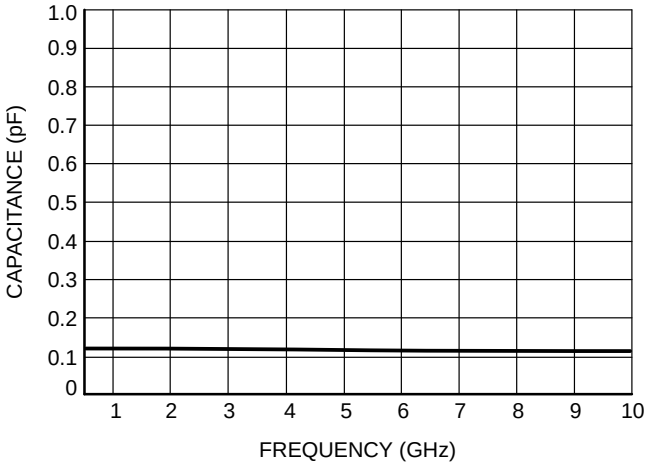


Figure 9. ESD8451MUT5G Capacitance over Frequency

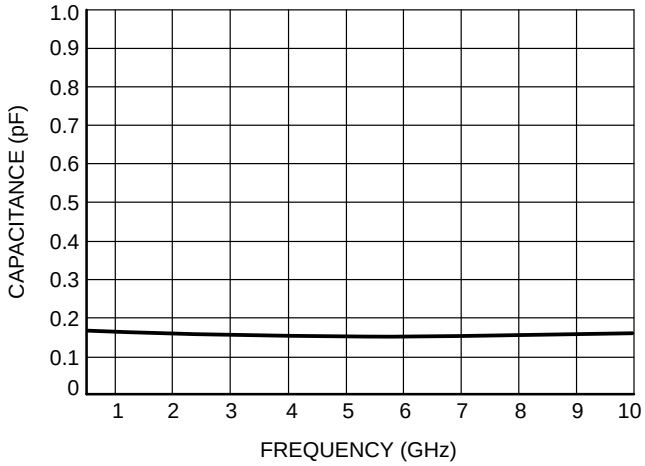


Figure 10. ESD8451N2T5G Capacitance over Frequency

TYPICAL CHARACTERISTICS

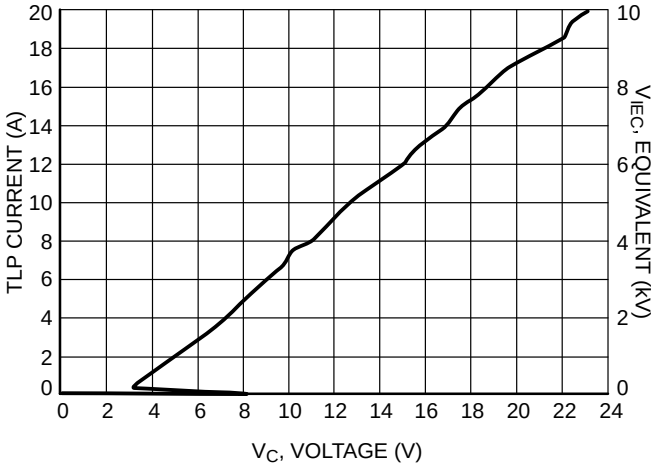


Figure 11. ESD8451MUT5G Positive TLP I−V Curve

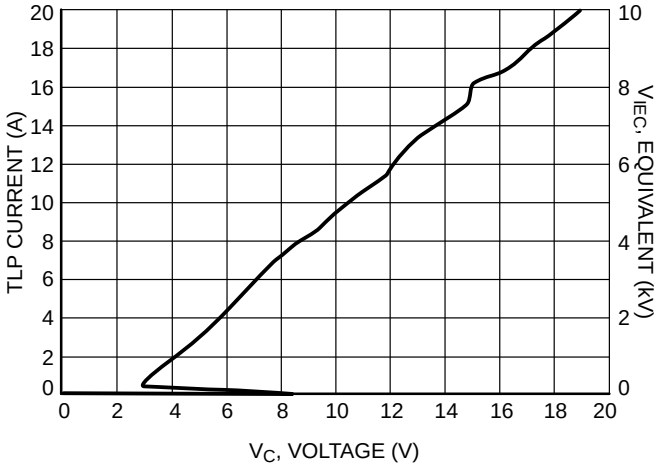


Figure 12. ESD8451N2T5G Positive TLP I−V Curve

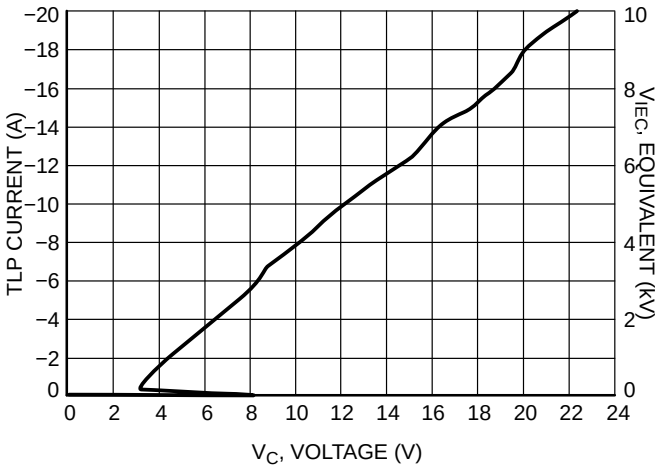


Figure 13. ESD8451MUT5G Negative TLP I−V Curve

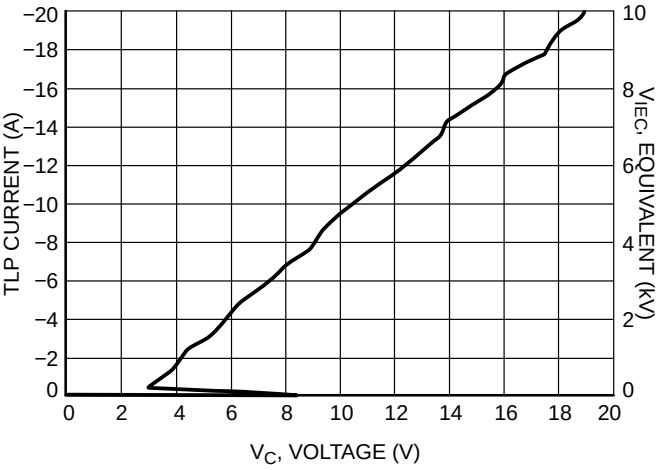
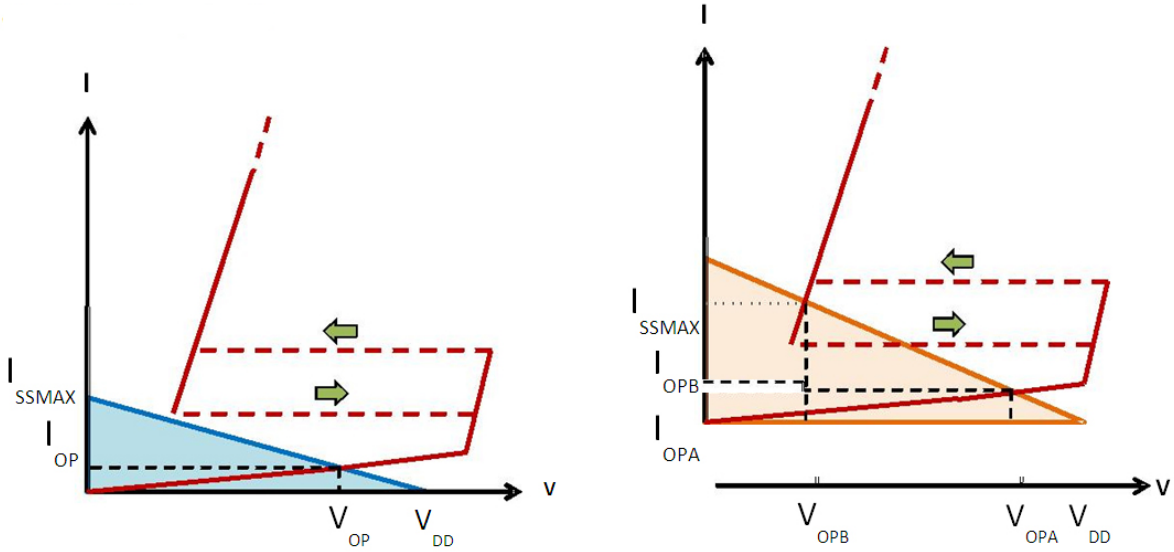


Figure 14. ESD8451N2T5G Negative TLP I−V Curve

Latch−Up Considerations

ON Semiconductor's 8000 series of ESD protection devices utilize a snap−back, SCR type structure. By using this technology, the potential for a latch−up condition was taken into account by performing load line analyses of common high speed serial interfaces. Example load lines for latch−up free applications and applications with the potential for latch−up are shown below with a generic IV characteristic of a snapback, SCR type structured device overlaid on each. In the latch−up free load line case, the IV characteristic of the snapback protection device intersects the load−line in one unique point (V_{OP}, I_{OP}). This is the only stable operating point of the circuit and the system is therefore latch−up free. In the non−latch up free load line case, the IV characteristic of the snapback protection device intersects the load−line in two points (V_{OPA}, I_{OPA}) and (V_{OPB}, I_{OPB}). Therefore in this case, the potential for latch−up exists if the system settles at (V_{OPB}, I_{OPB}) after a transient. Because of this, ESD8451 should not be used for HDMI applications – ESD8104 or ESD8040 have been designed to be acceptable for HDMI applications without latch−up. Please refer to Application Note AND9116/D for a more in−depth explanation of latch−up considerations using ESD8000 series devices.



ESD8451 Latch – up free:
USB 2.0 LS/FS, USB 2.0 HS,
USB 3.0 SS, DisplayPort

ESD8451 Potential Latch – up:
HDMI 1.4/1.3a TMDS

Figure 15. Example Load Lines for Latch−up Free Applications and Applications with the Potential for Latch−up

Table 1. SUMMARY OF SCR REQUIREMENTS FOR LATCH−UP FREE APPLICATIONS

Application	VBR (min) (V)	IH (min) (mA)	VH (min) (V)	ON Semiconductor ESD8000 Series Recommended PN
HDMI 1.4/1.3a TMDS	3.465	54.78	1.0	ESD8104, ESD8040
USB 2.0 LS/FS	3.301	1.76	1.0	ESD8004, ESD8451
USB 2.0 HS	0.482	N/A	1.0	ESD8004, ESD8451
USB 3.0 SS	2.800	N/A	1.0	ESD8004, ESD8006, ESD8451
DisplayPort	3.600	25.00	1.0	ESD8004, ESD8006, ESD8451

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

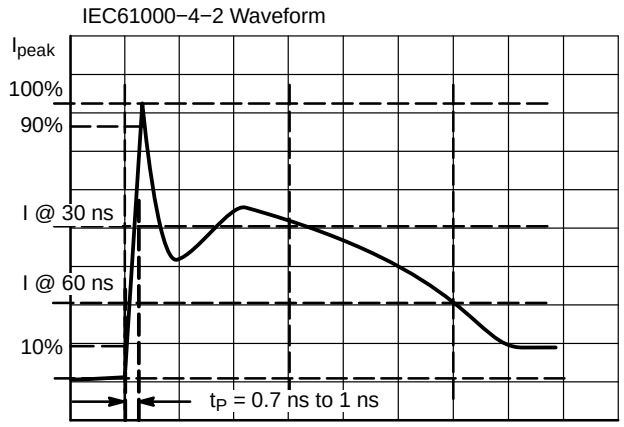


Figure 16. IEC61000−4−2 Spec

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 17. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 18 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

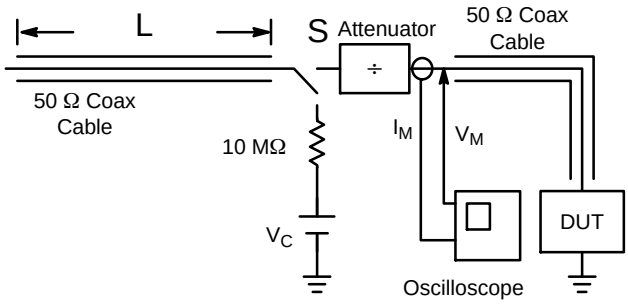


Figure 17. Simplified Schematic of a Typical TLP System

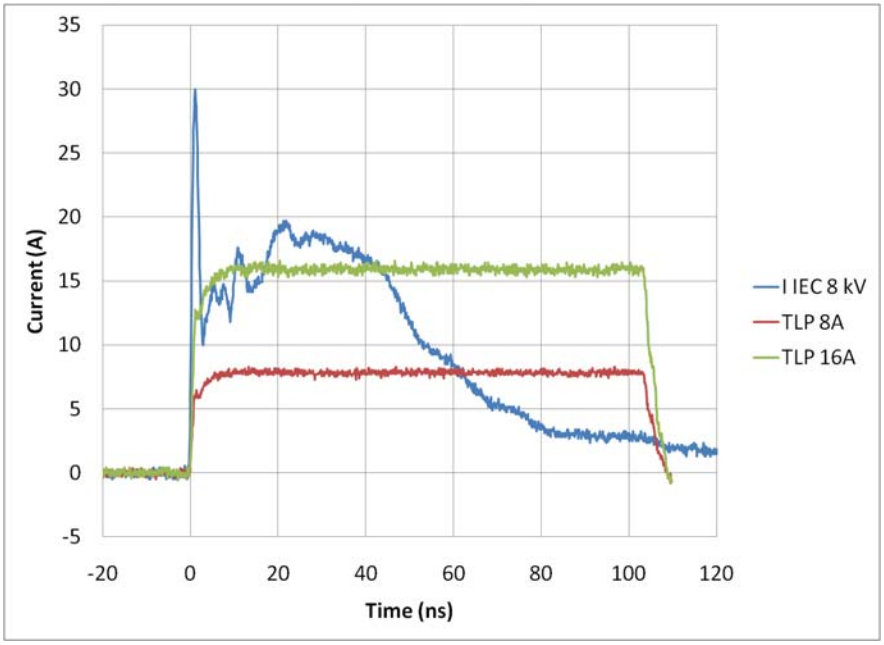


Figure 18. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms

ORDERING INFORMATION

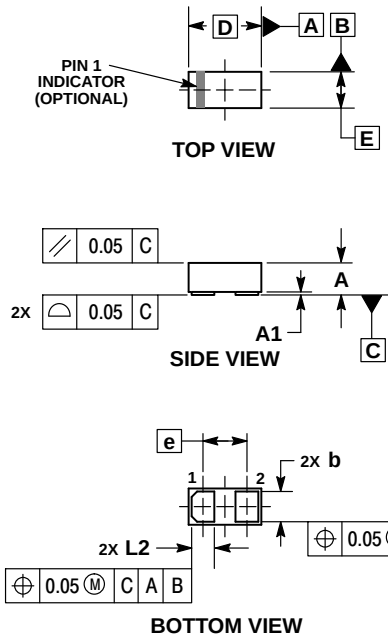
Device	Package	Shipping†
ESD8451N2T5G, SZESD8451N2T5G*	XDFN2 (Pb−Free)	8000 / Tape & Reel
ESD8451MUT5G	X3DFN2 (Pb−Free)	10000 / Tape & Reel
SZESD8451MUT5G*	X3DFN2 (Pb−Free)	15000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable.

PACKAGE DIMENSIONS

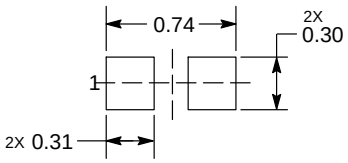
X3DFN2, 0.62x0.32, 0.355P, (0201)
CASE 152AF
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.25	0.33
A1	−−−	0.05
b	0.22	0.28
D	0.58	0.66
E	0.28	0.36
e	0.355 BSC	
L2	0.17	0.23

RECOMMENDED MOUNTING FOOTPRINT*



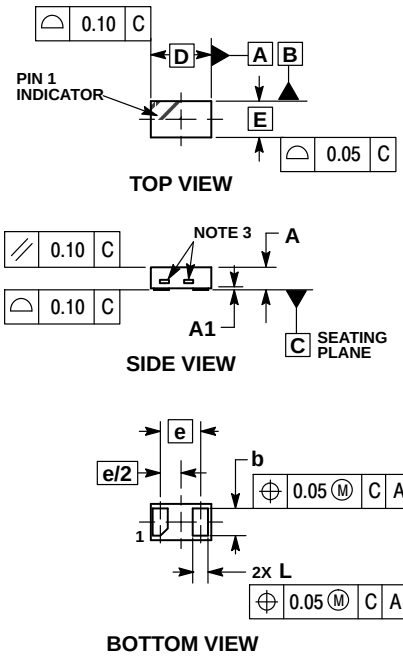
DIMENSIONS: MILLIMETERS

See Application Note AND8398/D for more mounting details

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

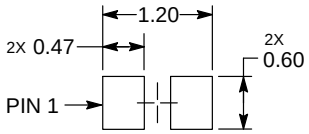
XDFN2 1.0x0.6, 0.65P (SOD−882)
CASE 711AM
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. EXPOSED COPPER ALLOWED AS SHOWN.

	MILLIMETERS	
DIM	MIN	MAX
A	0.34	0.44
A1	−−−	0.05
b	0.43	0.53
D	1.00 BSC	
E	0.60 BSC	
e	0.65 BSC	
L	0.20	0.30

RECOMMENDED SOLDER FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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