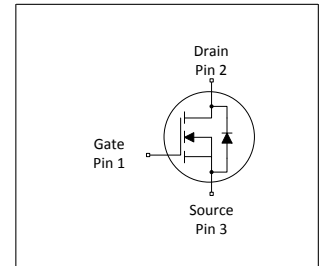


MOSFET

500V CoolMOS™ CE Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ CE is a price-performance optimized platform enabling to target cost sensitive applications in Consumer and Lighting markets by still meeting highest efficiency standards. The new series provides all benefits of a fast switching Superjunction MOSFET while not sacrificing ease of use and offering the best cost down performance ratio available on the market.



Features

- Extremely low losses due to very low FOM $R_{DS(on)} \cdot Q_g$ and E_{oss}
- Very high commutation ruggedness
- Easy to use/drive
- Pb-free plating, Halogen free mold compound
- Qualified for standard grade applications

Applications

PFC stages, hard switching PWM stages and resonant switching stages for e.g. PC Silverbox, Adapter, LCD & PDP TV and indoor lighting.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended



Table 1 Key Performance Parameters

| Parameter | Value | Unit |
|----------------------|-------|----------|
| $V_{DS} @ T_{j,max}$ | 550 | V |
| $R_{DS(on),max}$ | 1.4 | Ω |
| I_D | 4.8 | A |
| $Q_{g,typ}$ | 8.2 | nC |
| $I_{D,pulse}$ | 8.8 | A |
| $E_{oss}@400V$ | 0.79 | μJ |

| Type / Ordering Code | Package | Marking | Related Links |
|----------------------|-----------|----------|----------------|
| IPD50R1K4CE | PG-TO 252 | 50S1K4CE | see Appendix A |
| IPU50R1K4CE | PG-TO 251 | | |

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500V CoolMOS™ CE Power Transistor

IPD50R1K4CE, IPU50R1K4CE

1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|----------------|------------|------|------------|------------------|--|
| | | Min. | Typ. | Max. | | |
| Continuous drain current ¹⁾ | I_D | - | - | 4.8 3.1 | A | $T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$ |
| Pulsed drain current ²⁾ | $I_{D,pulse}$ | - | - | 8.8 | A | $T_C = 25^\circ\text{C}$ |
| Avalanche energy, single pulse | E_{AS} | - | - | 49 | mJ | $I_D = 1.1\text{A}$; $V_{DD} = 50\text{V}$ |
| Avalanche energy, repetitive | E_{AR} | - | - | 0.07 | mJ | $I_D = 1.1\text{A}$; $V_{DD} = 50\text{V}$ |
| Avalanche current, repetitive | I_{AR} | - | - | 1.1 | A | - |
| MOSFET dv/dt ruggedness | dv/dt | - | - | 50 | V/ns | $V_{DS} = 0 \dots 400\text{V}$ |
| Gate source voltage | V_{GS} | -20 -30 | - | 20 30 | V | static; AC ($f > 1\text{ Hz}$) |
| Power dissipation (non FullPAK) TO-252, TO-251 | P_{tot} | - | - | 42 | W | $T_C = 25^\circ\text{C}$ |
| Operating and storage temperature | T_j, T_{stg} | -55 | - | 150 | $^\circ\text{C}$ | - |
| Continuous diode forward current | I_S | - | - | 3.4 | A | $T_C = 25^\circ\text{C}$ |
| Diode pulse current ²⁾ | $I_{S,pulse}$ | - | - | 8.8 | A | $T_C = 25^\circ\text{C}$ |
| Reverse diode dv/dt ³⁾ | dv/dt | - | - | 15 | V/ns | $V_{DS} = 0 \dots 400\text{V}$, $I_{SD} \leq I_S$, $T_j = 25^\circ\text{C}$, $t_{cond} < 2\mu\text{s}$ |
| Maximum diode commutation speed ³⁾ | di/dt | - | - | 500 | A/ μs | $V_{DS} = 0 \dots 400\text{V}$, $I_{SD} \leq I_S$, $T_j = 25^\circ\text{C}$, $t_{cond} < 2\mu\text{s}$ |

2 Thermal characteristics

Table 3 Thermal characteristics DPAK, IPAK

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|------------|--------|------|----------|--------------------|--|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case | R_{thJC} | - | - | 2.95 | $^\circ\text{C/W}$ | - |
| Thermal resistance, junction - ambient ⁴⁾ | R_{thJA} | - | - | 62 35 | $^\circ\text{C/W}$ | SMD version, device on PCB, minimal footprint SMD version, device on PCB, 6cm ² cooling area ⁴⁾ |
| Soldering temperature, wave- & reflowsoldering allowed | T_{sold} | - | - | 260 | $^\circ\text{C}$ | reflow MSL 1 |

¹⁾ Limited by $T_{j,max}$. Maximum duty cycle $D=0.5$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ $V_{DClink}=400\text{V}$; $V_{DS,peak} < V_{(BR)DSS}$; identical low side and high side switch with identical R_G

⁴⁾ Device on 40mm*40mm*1.5mm one layer epoxy PCB FR4 with 6cm² copper area (thickness 70 μm) for drain connection. PCB is vertical without air stream cooling.

3 Electrical characteristics

Table 4 Static characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|----------------------------------|---------------|--------|------|------|----------|---|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 500 | - | - | V | $V_{GS}=0V, I_D=1mA$ |
| Gate threshold voltage | $V_{(GS)th}$ | 2.50 | 3 | 3.50 | V | $V_{DS}=V_{GS}, I_D=0.07mA$ |
| Zero gate voltage drain current | I_{DSS} | - | - | 1 | μA | $V_{DS}=500V, V_{GS}=0V, T_j=25^\circ C$ $V_{DS}=500V, V_{GS}=0V, T_j=150^\circ C$ |
| Gate-source leakage current | I_{GSS} | - | - | 100 | nA | $V_{GS}=20V, V_{DS}=0V$ |
| Drain-source on-state resistance | $R_{DS(on)}$ | - | 1.26 | 1.40 | Ω | $V_{GS}=13V, I_D=0.9A, T_j=25^\circ C$ $V_{GS}=13V, I_D=0.9A, T_j=150^\circ C$ |
| Gate resistance | R_G | - | 7 | - | Ω | $f=1\text{ MHz, open drain}$ |

Table 5 Dynamic characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|--------------|--------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Input capacitance | C_{iss} | - | 178 | - | pF | $V_{GS}=0V, V_{DS}=100V, f=1MHz$ |
| Output capacitance | C_{oss} | - | 11 | - | pF | $V_{GS}=0V, V_{DS}=100V, f=1MHz$ |
| Effective output capacitance, energy related ¹⁾ | $C_{o(er)}$ | - | 10 | - | pF | $V_{GS}=0V, V_{DS}=0...400V$ |
| Effective output capacitance, time related ²⁾ | $C_{o(tr)}$ | - | 36 | - | pF | $I_D=constant, V_{GS}=0V, V_{DS}=0...400V$ |
| Turn-on delay time | $t_{d(on)}$ | - | 6.5 | - | ns | $V_{DD}=400V, V_{GS}=13V, I_D=1.1A,$ $R_G=5.3\Omega$ |
| Rise time | t_r | - | 6 | - | ns | $V_{DD}=400V, V_{GS}=13V, I_D=1.1A,$ $R_G=5.3\Omega$ |
| Turn-off delay time | $t_{d(off)}$ | - | 23 | - | ns | $V_{DD}=400V, V_{GS}=13V, I_D=1.1A,$ $R_G=5.3\Omega$ |
| Fall time | t_f | - | 30 | - | ns | $V_{DD}=400V, V_{GS}=13V, I_D=1.1A,$ $R_G=5.3\Omega$ |

Table 6 Gate charge characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-----------------------|---------------|--------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Gate to source charge | Q_{gs} | - | 1 | - | nC | $V_{DD}=400V, I_D=1.1A, V_{GS}=0\text{ to }10V$ |
| Gate to drain charge | Q_{gd} | - | 4.6 | - | nC | $V_{DD}=400V, I_D=1.1A, V_{GS}=0\text{ to }10V$ |
| Gate charge total | Q_g | - | 8.2 | - | nC | $V_{DD}=400V, I_D=1.1A, V_{GS}=0\text{ to }10V$ |
| Gate plateau voltage | $V_{plateau}$ | - | 5.4 | - | V | $V_{DD}=400V, I_D=1.1A, V_{GS}=0\text{ to }10V$ |

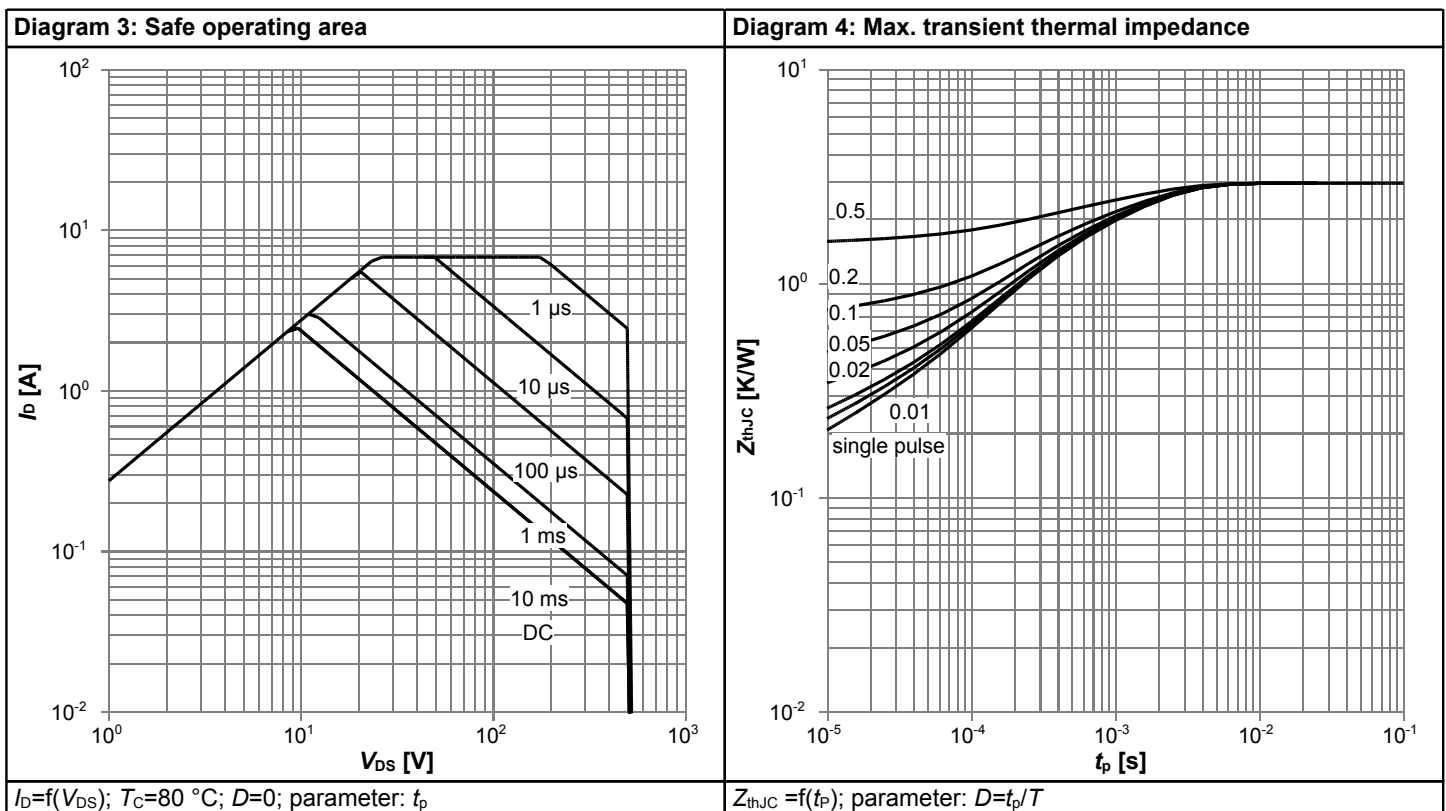
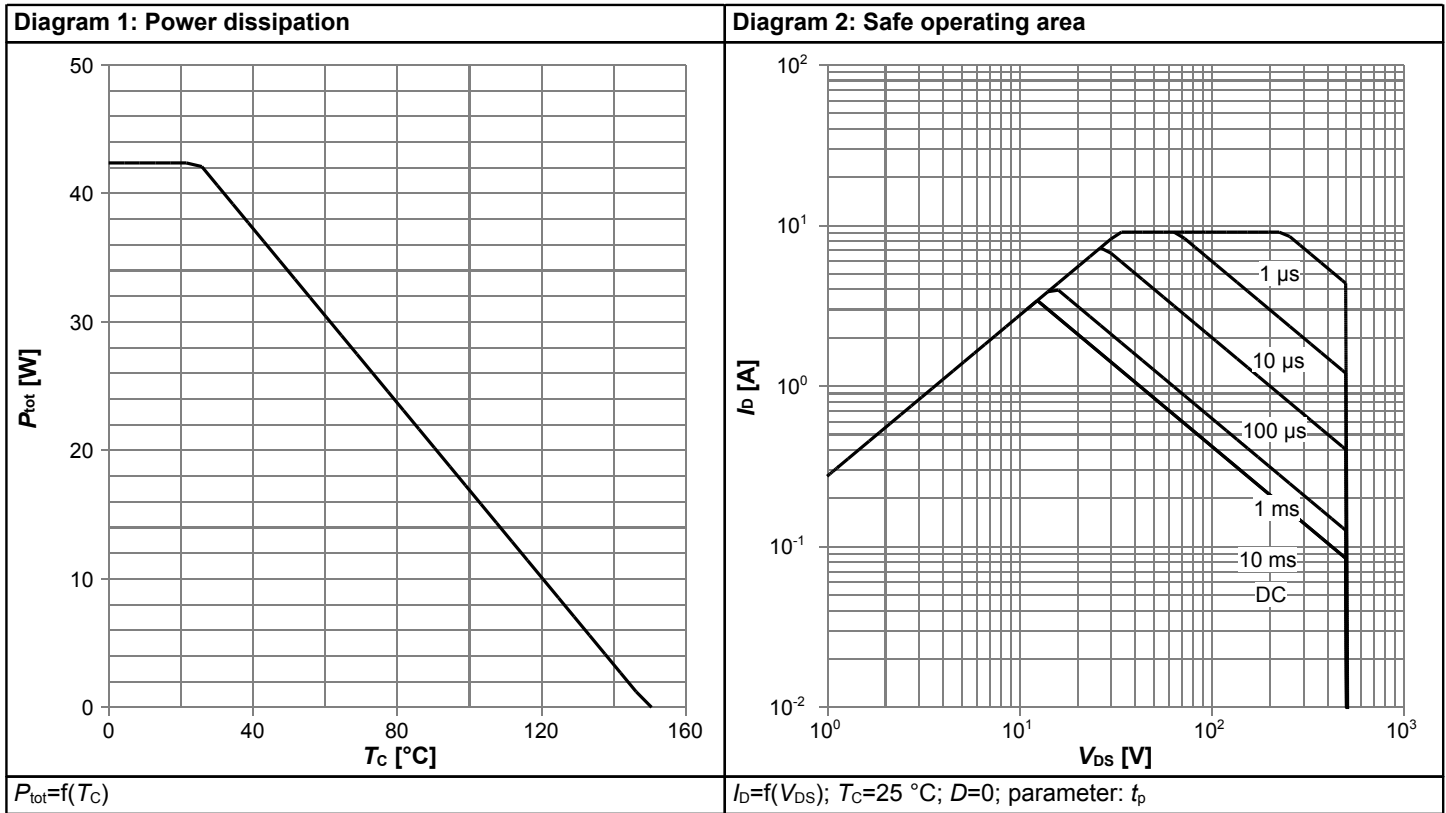
¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

Table 7 Reverse diode characteristics

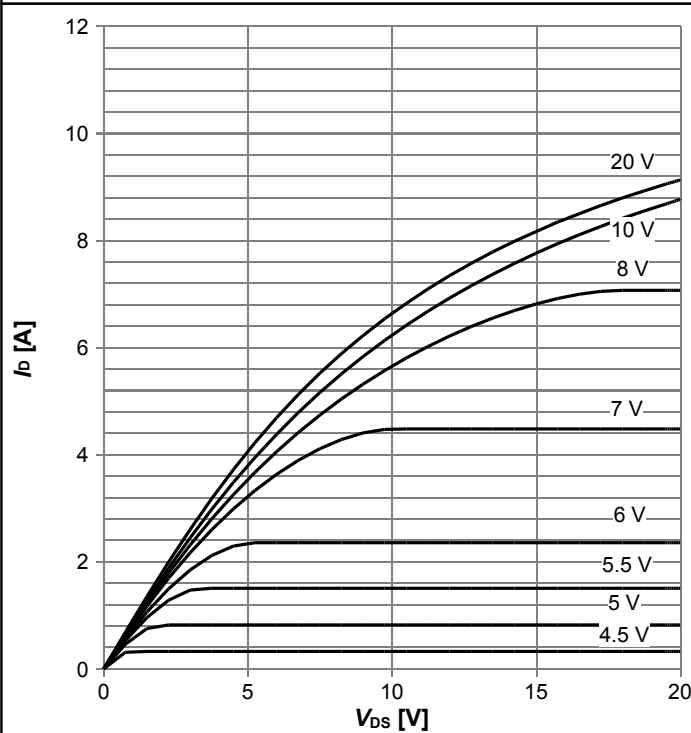
| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-------------------------------|-----------|--------|------|------|---------|--|
| | | Min. | Typ. | Max. | | |
| Diode forward voltage | V_{SD} | - | 0.83 | - | V | $V_{GS}=0V, I_F=1.1A, T_i=25^{\circ}C$ |
| Reverse recovery time | t_{rr} | - | 120 | - | ns | $V_R=400V, I_F=1.1A, di_F/dt=100A/\mu s$ |
| Reverse recovery charge | Q_{rr} | - | 0.5 | - | μC | $V_R=400V, I_F=1.1A, di_F/dt=100A/\mu s$ |
| Peak reverse recovery current | I_{rrm} | - | 6.8 | - | A | $V_R=400V, I_F=1.1A, di_F/dt=100A/\mu s$ |

4 Electrical characteristics diagrams



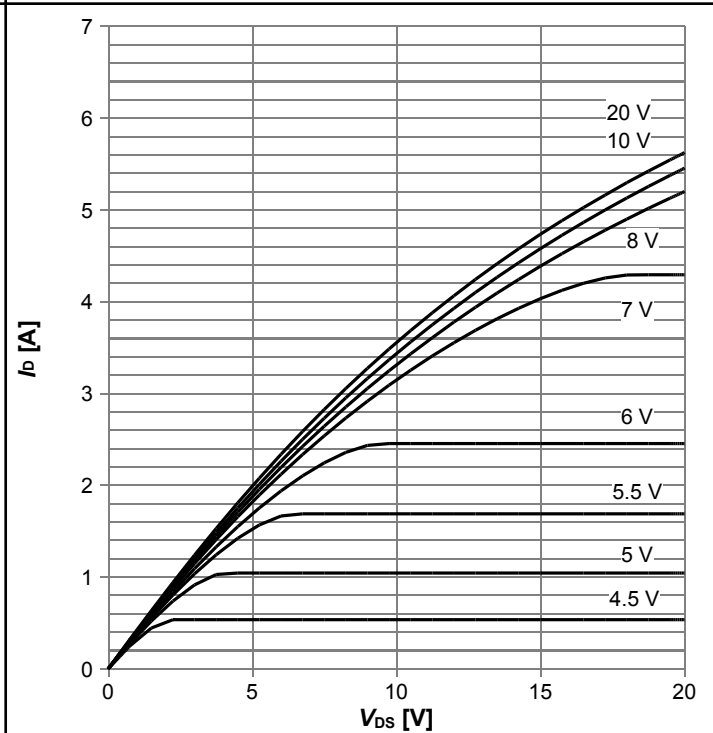
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IPD50R1K4CE, IPU50R1K4CE

Diagram 5: Typ. output characteristics $T_j=25^\circ\text{C}$



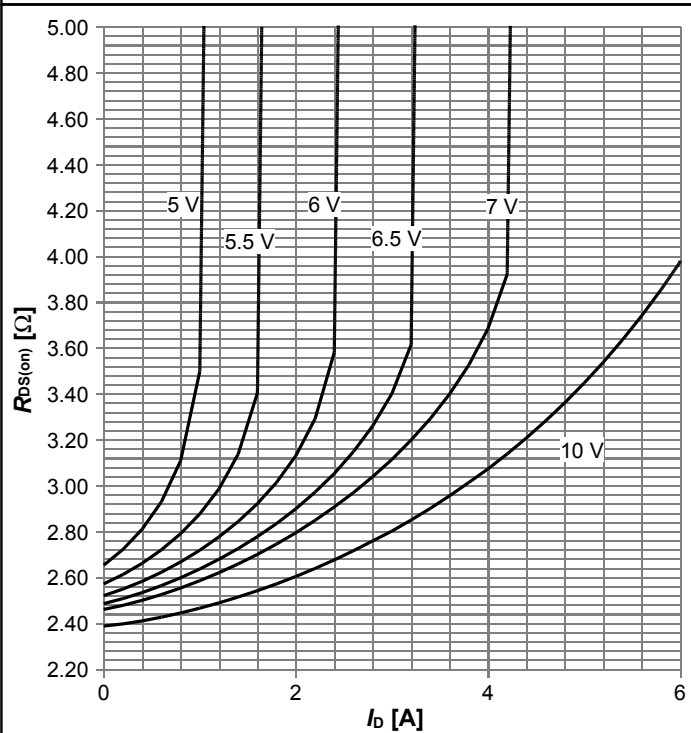
$I_D=f(V_{DS}); T_j=25^\circ\text{C};$ parameter: V_{GS}

Diagram 6: Typ. output characteristics $T_j=125^\circ\text{C}$



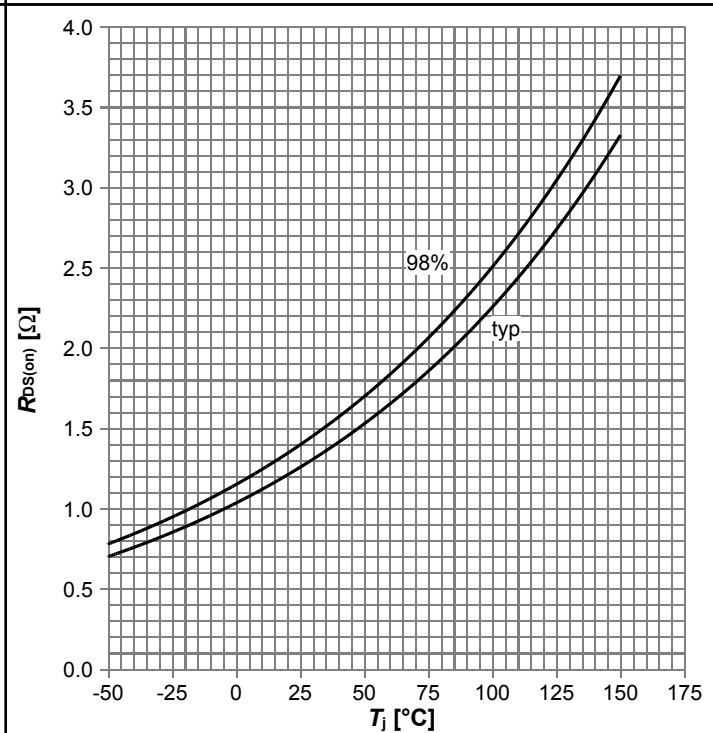
$I_D=f(V_{DS}); T_j=125^\circ\text{C};$ parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



$R_{DS(on)}=f(I_D); T_j=125^\circ\text{C};$ parameter: V_{GS}

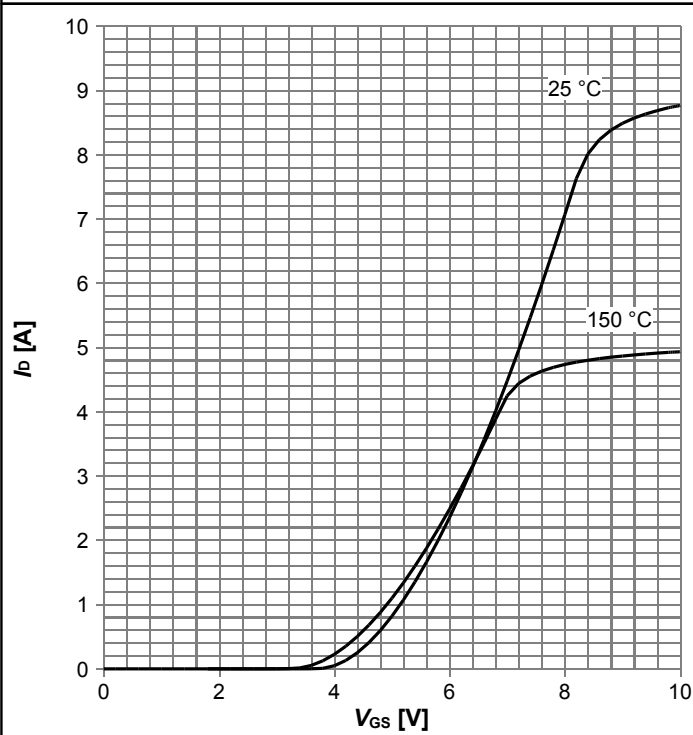
Diagram 8: Drain-source on-state resistance



$R_{DS(on)}=f(T_j); I_D=0.9\text{ A}; V_{GS}=13\text{ V}$

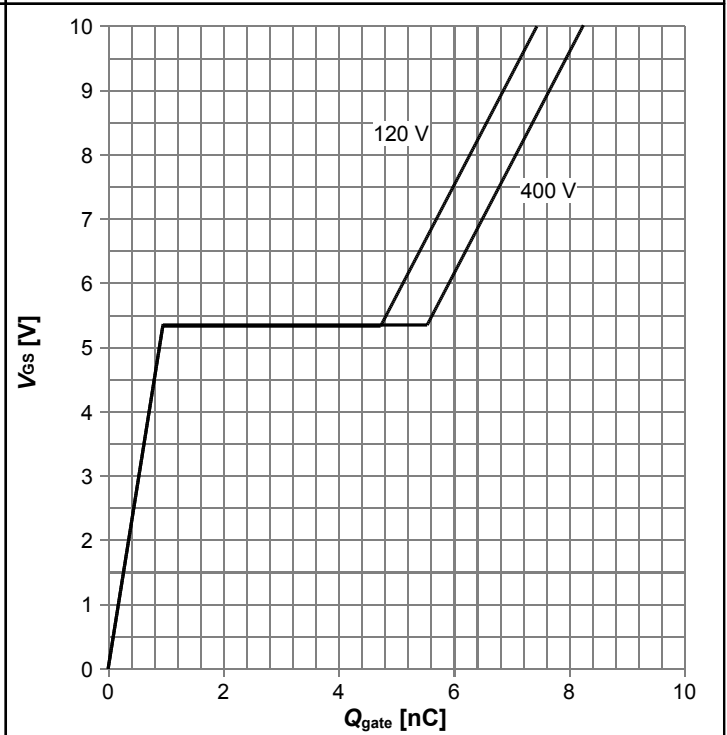
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Diagram 9: Typ. transfer characteristics



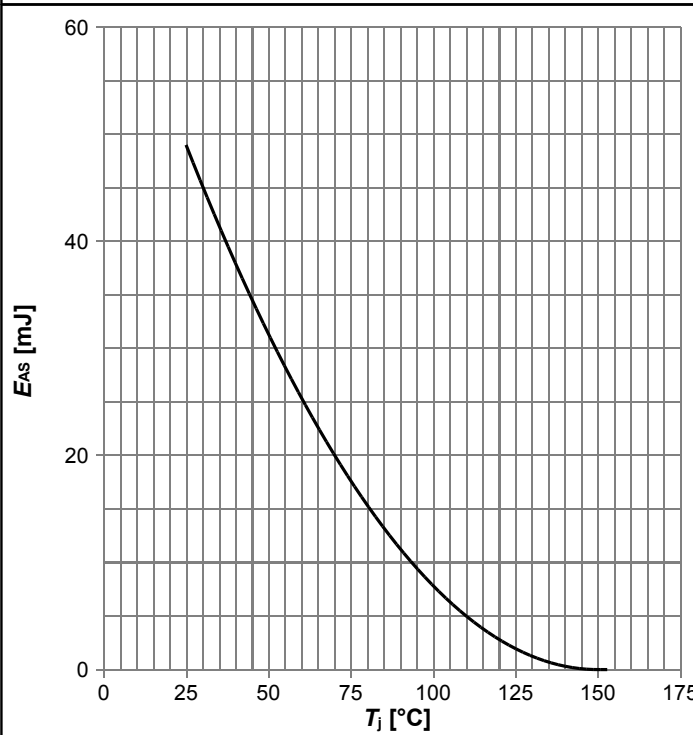
$I_D = f(V_{GS}); V_{DS} = 20V; \text{parameter: } T_j$

Diagram 10: Typ. gate charge



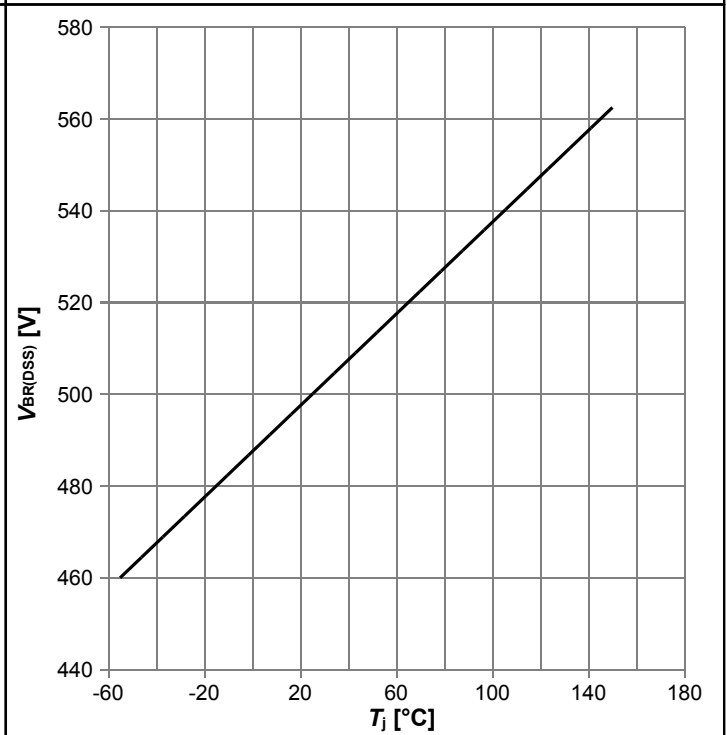
$V_{GS} = f(Q_{gate}); I_D = 1.1 \text{ A pulsed}; \text{parameter: } V_{DD}$

Diagram 11: Avalanche energy



$E_{AS} = f(T_j); I_D = 1.1 \text{ A}; V_{DD} = 50 \text{ V}$

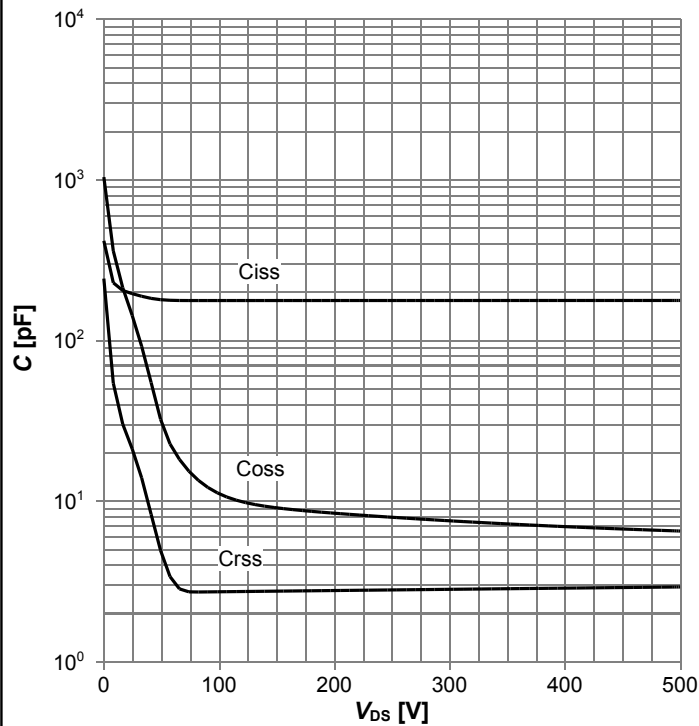
Diagram 12: Drain-source breakdown voltage



$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$

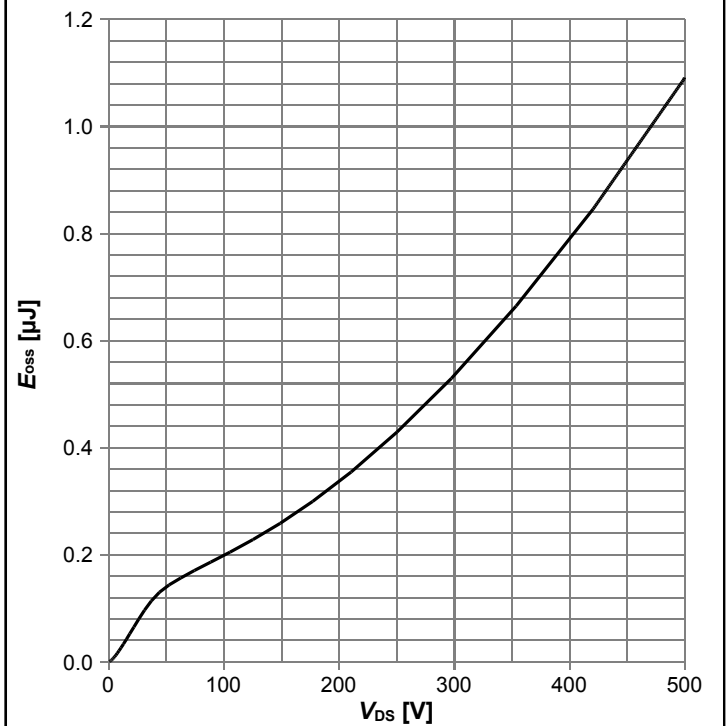
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Diagram 13: Typ. capacitances



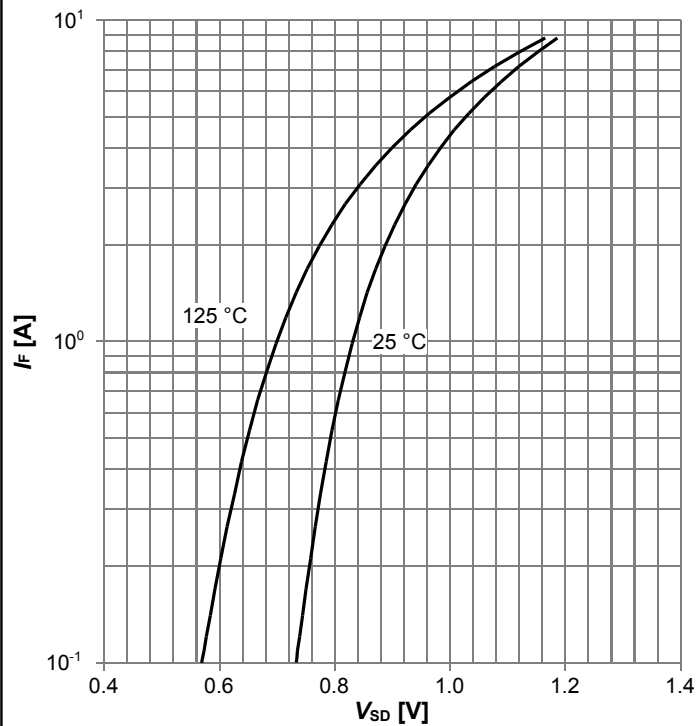
$C=f(V_{Ds}); V_{GS}=0\text{ V}; f=1\text{ MHz}$

Diagram 14: Typ. Coss stored energy



$E_{oss}=f(V_{Ds})$

Diagram 15: Forward characteristics of reverse diode



$I_F=f(V_{SD}); \text{parameter: } T_j$

5 Test Circuits

Table 8 Diode characteristics

| Test circuit for diode characteristics | Diode recovery waveform |
|--|-------------------------|
| | |

Table 9 Switching times

| Switching times test circuit for inductive load | Switching times waveform |
|---|--------------------------|
| | |

Table 10 Unclamped inductive load

| Unclamped inductive load test circuit | Unclamped inductive waveform |
|---------------------------------------|------------------------------|
| | |

6 Package Outlines



*) mold flash not included

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 2.16 | 2.41 | 0.085 | 0.095 |
| A1 | 0.00 | 0.15 | 0.000 | 0.006 |
| b | 0.64 | 0.89 | 0.025 | 0.035 |
| b2 | 0.65 | 1.15 | 0.026 | 0.045 |
| b3 | 5.00 | 5.50 | 0.197 | 0.217 |
| c | 0.46 | 0.60 | 0.018 | 0.024 |
| c2 | 0.46 | 0.98 | 0.018 | 0.039 |
| D | 5.97 | 6.22 | 0.235 | 0.245 |
| D1 | 5.02 | 5.84 | 0.198 | 0.230 |
| E | 6.40 | 6.73 | 0.252 | 0.265 |
| E1 | 4.70 | 5.60 | 0.185 | 0.220 |
| e | 2.29 (BSC) | | 0.090 (BSC) | |
| e1 | 4.57 (BSC) | | 0.180 (BSC) | |
| N | 3 | | 3 | |
| H | 9.40 | 10.48 | 0.370 | 0.413 |
| L | 1.18 | 1.70 | 0.046 | 0.067 |
| L3 | 0.90 | 1.25 | 0.035 | 0.049 |
| L4 | 0.51 | 1.00 | 0.020 | 0.039 |
| F1 | 10.60 | | 0.417 | |
| F2 | 6.40 | | 0.252 | |
| F3 | 2.20 | | 0.087 | |
| F4 | 5.80 | | 0.228 | |
| F5 | 5.76 | | 0.227 | |
| F6 | 1.20 | | 0.047 | |

| |
|------------------------------------|
| DOCUMENT NO. Z8B00003328 |
| SCALE 0 2.0 4mm |
| EUROPEAN PROJECTION |
| ISSUE DATE 01-09-2015 |
| REVISION 05 |

Figure 1 Outline PG-TO 252, dimensions in mm/inches

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IPD50R1K4CE, IPU50R1K4CE

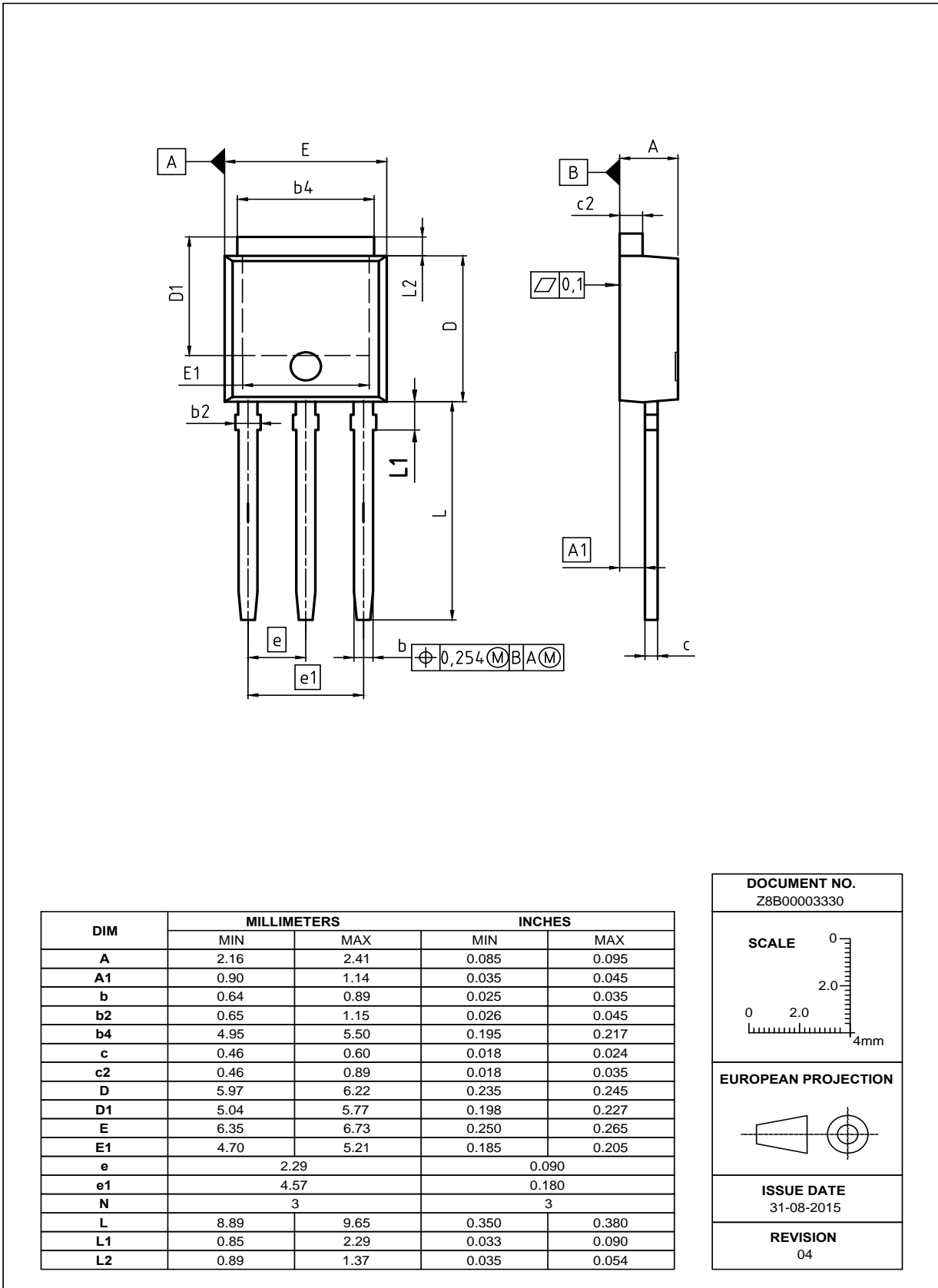


Figure 2 Outline PG-TO 251, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- IFX CoolMOS Webpage: www.infineon.com
- IFX Design tools: www.infineon.com

500V CoolMOS™ CE Power Transistor

IPD50R1K4CE, IPU50R1K4CE

Revision History

IPD50R1K4CE, IPU50R1K4CE

Revision: 2016-06-13, Rev. 2.4

Previous Revision

| Revision | Date | Subjects (major changes since last revision) |
|----------|------------|---|
| 2.0 | 2012-09-13 | Release of final version |
| 2.1 | 2012-12-05 | release of final datasheet |
| 2.2 | 2013-07-16 | update to Halogen free mold compound |
| 2.3 | 2015-11-17 | Updated to standard grade qualified & updated package drawing |
| 2.4 | 2016-06-13 | Updated ID ratings, Zth, SOA and Pd curves |

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