BTN8962TA

High Current PN Half Bridge
NovalithIC™

Data Sheet

Rev. 1.0, 2013-05-17

Automotive Power

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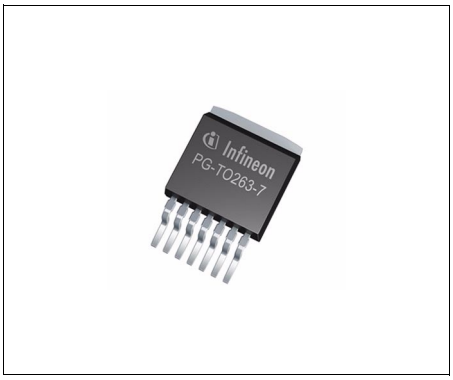
1 Overview



PG-TO263-7-1

Features

- Path resistance of max. 30.3 mΩ @ 150 °C (typ. 14.2 mΩ @ 25 °C)
  High Side: max. 13.4 mΩ @ 150 °C (typ. 6.7 mΩ @ 25 °C)
  Low Side: max. 16.9 mΩ @ 150 °C (typ. 7.5 mΩ @ 25 °C)
- Enhanced switching speed for reduced switching losses
- Capable for high PWM frequency combined with active freewheeling
- Low quiescent current of typ. 7 µA @ 25 °C
- Switched mode current limitation for reduced power dissipation in overcurrent
- Current limitation level of 30 A min.
- Status flag diagnosis with current sense capability
- Overtemperature shut down with latch behaviour
- Undervoltage shut down
- Driver circuit with logic level inputs
- Adjustable slew rates for optimized EMI
- Operation up to 40V
- Green Product (RoHS compliant)
- AEC Qualified

Description

The BTN8962TA is an integrated high current half bridge for motor drive applications. It is part of the NovalithIC™ family containing one p-channel highside MOSFET and one n-channel lowside MOSFET with an integrated driver IC in one package. Due to the p-channel highside switch the need for a charge pump is eliminated thus minimizing EMI. Interfacing to a microcontroller is made easy by the integrated driver IC which features logic level inputs, diagnosis with current sense, slew rate adjustment, dead time generation and protection against overtemperature, undervoltage, overcurrent and short circuit.

The BTN8962TA provides a cost optimized solution for protected high current PWM motor drives with very low board space consumption.

Type	Package	Marking
BTN8962TA	PG-TO263-7-1	BTN8962TA

2 Block Diagram

The BTN8962TA is part of the NovalithIC™ family containing three separate chips in one package: One p-channel highside MOSFET and one n-channel lowside MOSFET together with a driver IC, forming an integrated high current half-bridge. All three chips are mounted on one common lead frame, using the chip on chip and chip by chip technology. The power switches utilize vertical MOS technologies to ensure optimum on state resistance. Due to the p-channel highside switch the need for a charge pump is eliminated thus minimizing EMI. Interfacing to a microcontroller is made easy by the integrated driver IC which features logic level inputs, diagnosis with current sense, slew rate adjustment, dead time generation and protection against overtemperature, undervoltage, overcurrent and short circuit. The BTN8962TA can be combined with other BTN8962TA to form H-bridge and 3-phase drive configurations.

2.1 Block Diagram

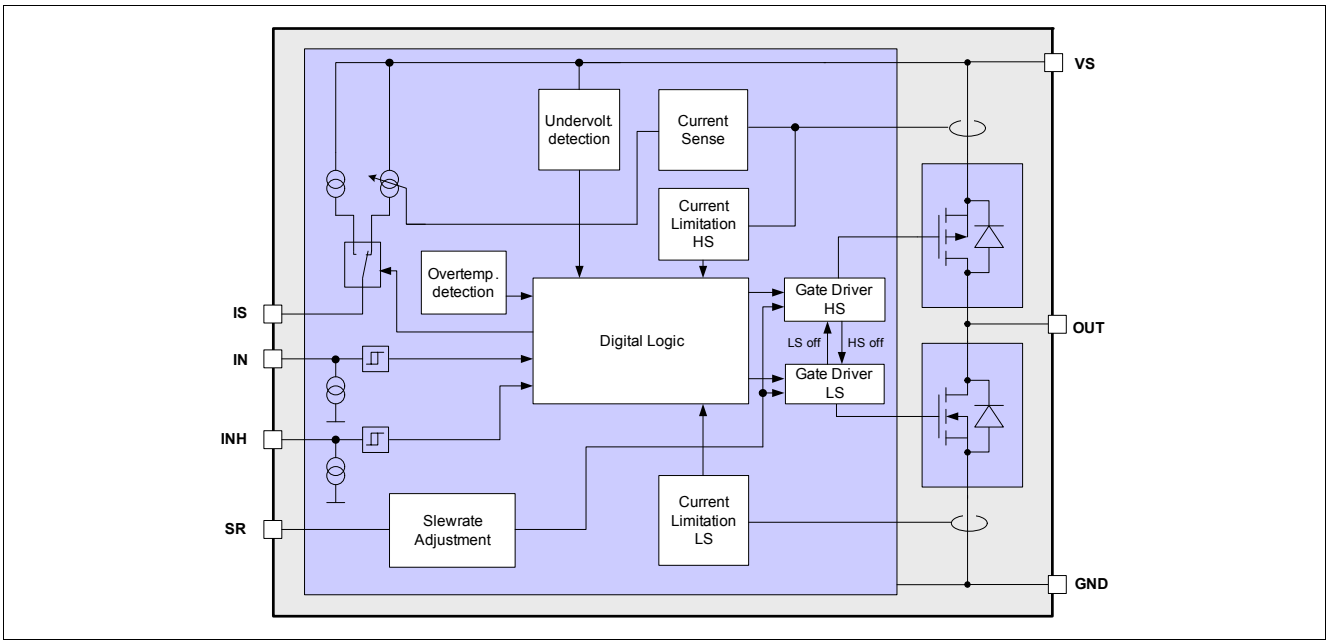


Figure 1 Block Diagram

2.2 Terms

Following figure shows the terms used in this data sheet.

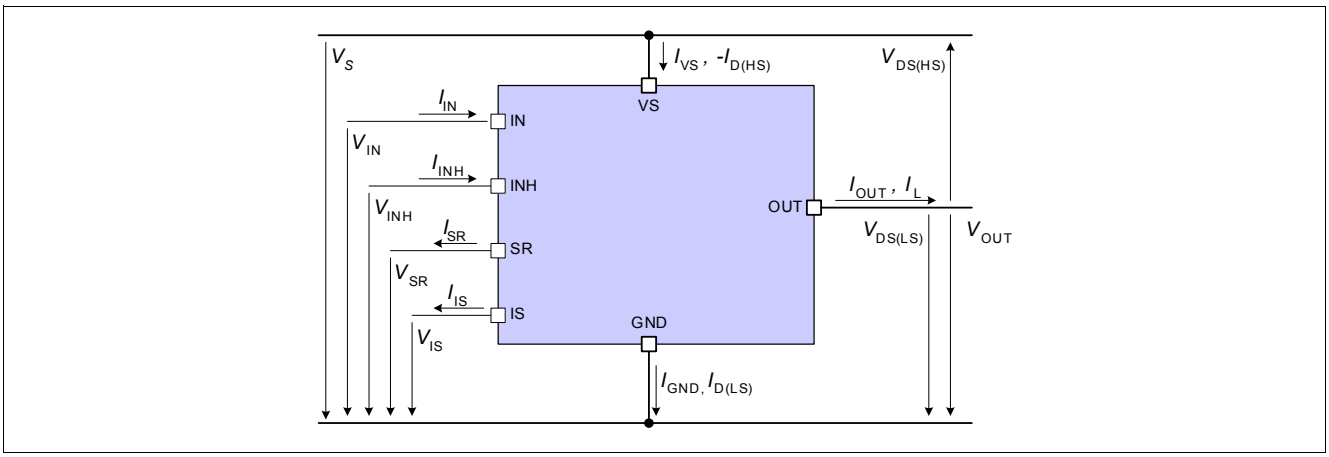


Figure 2 Terms

3 Pin Configuration

3.1 Pin Assignment

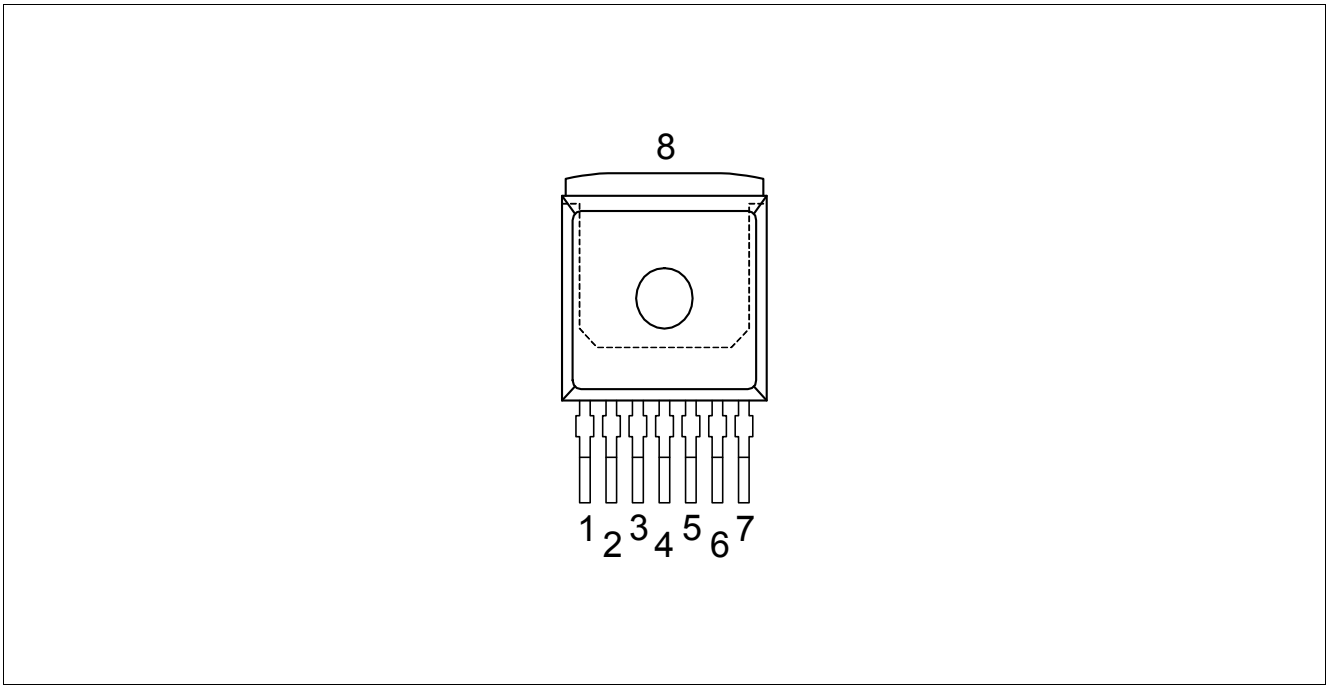


Figure 3 Pin Assignment BTN8962TA (top view)

3.2 Pin Definitions and Functions

Pin	Symbol	I/O	Function
1	**GND**	**-**	**Ground**
2	IN	I	Input Defines whether high- or lowside switch is activated
3	INH	I	Inhibit When set to low device goes in sleep mode
4,8	**OUT**	**O**	**Power output of the bridge**
5	SR	I	Slew Rate The slew rate of the power switches can be adjusted by connecting a resistor between SR and GND
6	IS	O	Current Sense and Diagnostics
7	**VS**	**-**	**Supply**

Bold type: pin needs power wiring

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Voltages						
4.1.1	Supply Voltage	V_S	-0.3	40	V	–
4.1.2	Drain-Source Voltage High Side	$V_{DS(HS)}$	-40	–	V	$T_j \geq 25$°C
			-38	–	V	$T_j < 25$°C
4.1.3	Drain-Source Voltage Low Side	$V_{DS(LS)}$	–	40	V	$T_j \geq 25$°C
			–	38	V	$T_j < 25$°C
4.1.4	Logic Input Voltage	V_{IN} V_{INH}	-0.3	5.3	V	–
4.1.5	Voltage at SR Pin	V_{SR}	-0.3	1.0	V	–
4.1.6	Voltage between VS and IS Pin	V_S -V_{IS}	-0.3	40	V	–
4.1.7	Voltage at IS Pin	V_{IS}	-20	40	V	–
Currents						
4.1.8	HS/LS Continuous Drain Current[2)]	$I_{D(HS)}$ $I_{D(LS)}$	-30	30	A	$T_C < 85$°C switch active
			-27	27	A	$T_C < 125$°C switch active
4.1.9	HS/LS Pulsed Drain Current[2)]	$I_{D(HS)}$ $I_{D(LS)}$	 -70 -63	 70 63	A	t_{pulse} = 10ms single pulse $T_C < 85$°C $T_C < 125$°C
4.1.10	HS/LS PWM Current[2)]	$I_{D(HS)}$ $I_{D(LS)}$	 -40 -36	 40 36	A	f = 1kHz, DC = 50% $T_C < 85$°C $T_C < 125$°C
			 -42 -37	 42 37	A	f = 20kHz, DC = 50% $T_C < 85$°C $T_C < 125$°C
Temperatures						
4.1.11	Junction Temperature	T_j	-40	150	°C	–
4.1.12	Storage Temperature	T_{stg}	-55	150	°C	–
ESD Susceptibility						
4.1.13	ESD Resistivity HBM IN, INH, SR, IS OUT, GND, VS	V_{ESD}	 -2 -6	 2 6	kV	HBM[3)]

1) Not subject to production test, specified by design

2) Maximum reachable current may be smaller depending on current limitation level

3) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS-001 (1,5kΩ, 100pF)

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

Maximum Single Pulse Current

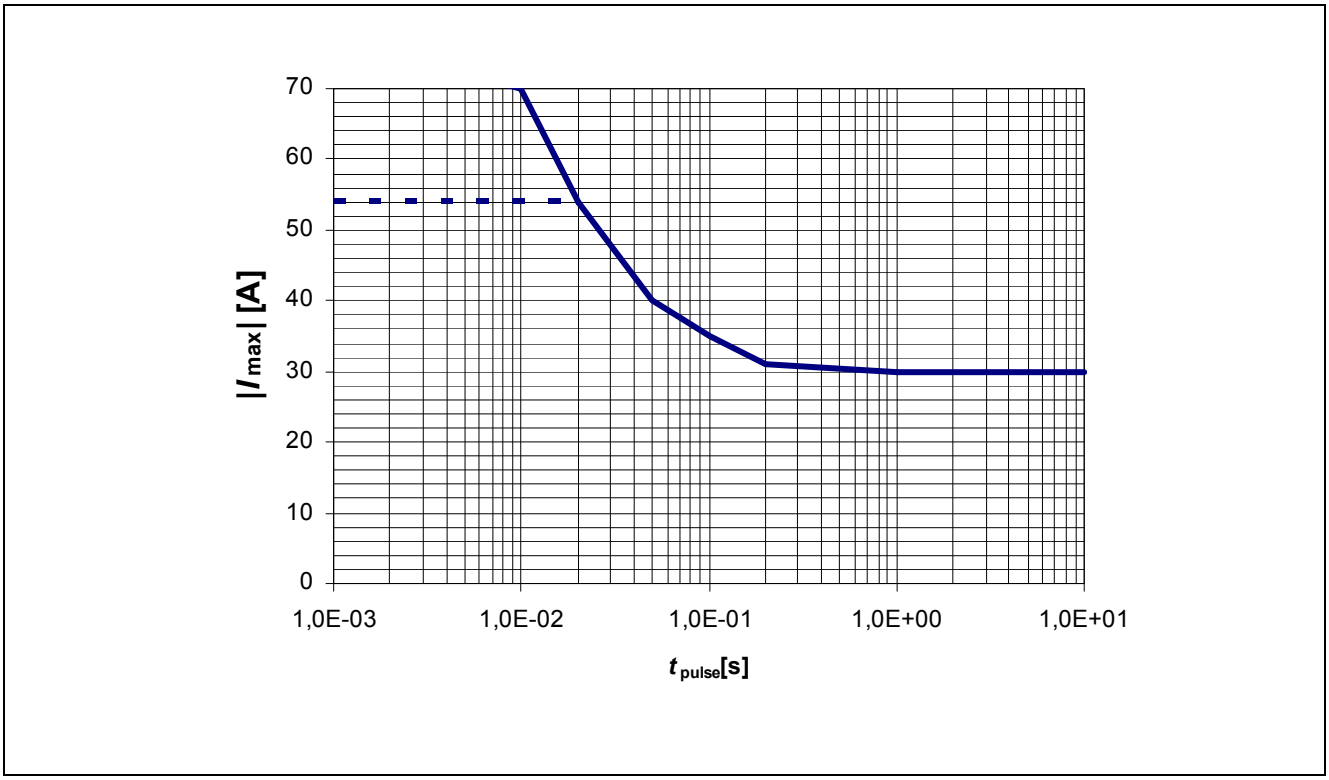


Figure 4 BTN8962TA Maximum Single Pulse Current (T_C < 85°C)

This diagram shows the maximum single pulse current that can be driven for a given pulse time t_{pulse}. The maximum reachable current may be smaller depending on the current limitation level. Pulse time may be limited due to thermal protection of the device.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Supply Voltage Range for Normal Operation	$V_{S(nor)}$	8	18	V	–
4.2.2	Extended Supply Voltage Range for Operation	$V_{S(ext)}$	5.5	40	V	Parameter Deviations possible
4.2.3	Junction Temperature	T_j	-40	150	°C	–

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

4.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Thermal Resistance Junction-Case, High Side Switch $R_{thjc(HS)} = \Delta T_{j(HS)} / P_{v(HS)}$	$R_{thJC(HS)}$	–	0.6	0.9	K/W	1)
4.3.2	Thermal Resistance Junction-Case, Low Side Switch $R_{thjc(LS)} = \Delta T_{j(LS)} / P_{v(LS)}$	$R_{thJC(LS)}$	–	1.7	2.4	K/W	1)
4.3.3	Thermal Resistance Junction-Ambient	R_{thJA}	–	20	–	K/W	1) 2)

1) Not subject to production test, specified by design

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

5 Block Description and Characteristics

5.1 Supply Characteristics

V_S = 8 V to 18 V, T_j = -40 °C to +150 °C, I_L = 0 A, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
General							
5.1.1	Supply Current	$I_{VS(on)}$	–	2.2	3.3	mA	V_{INH} = 5 V V_{IN} = 0 V or 5 V R_{SR} = 0 Ω DC-mode normal operation (no fault condition)
5.1.2	Quiescent Current	$I_{VS(off)}$	–	7	13	µA	V_{INH} = 0 V V_{IN} = 0 V or 5 V T_j < 85 °C 1)
			–	–	65	µA	V_{INH} = 0 V V_{IN} = 0 V or 5 V

1) Not subject to production test, specified by design

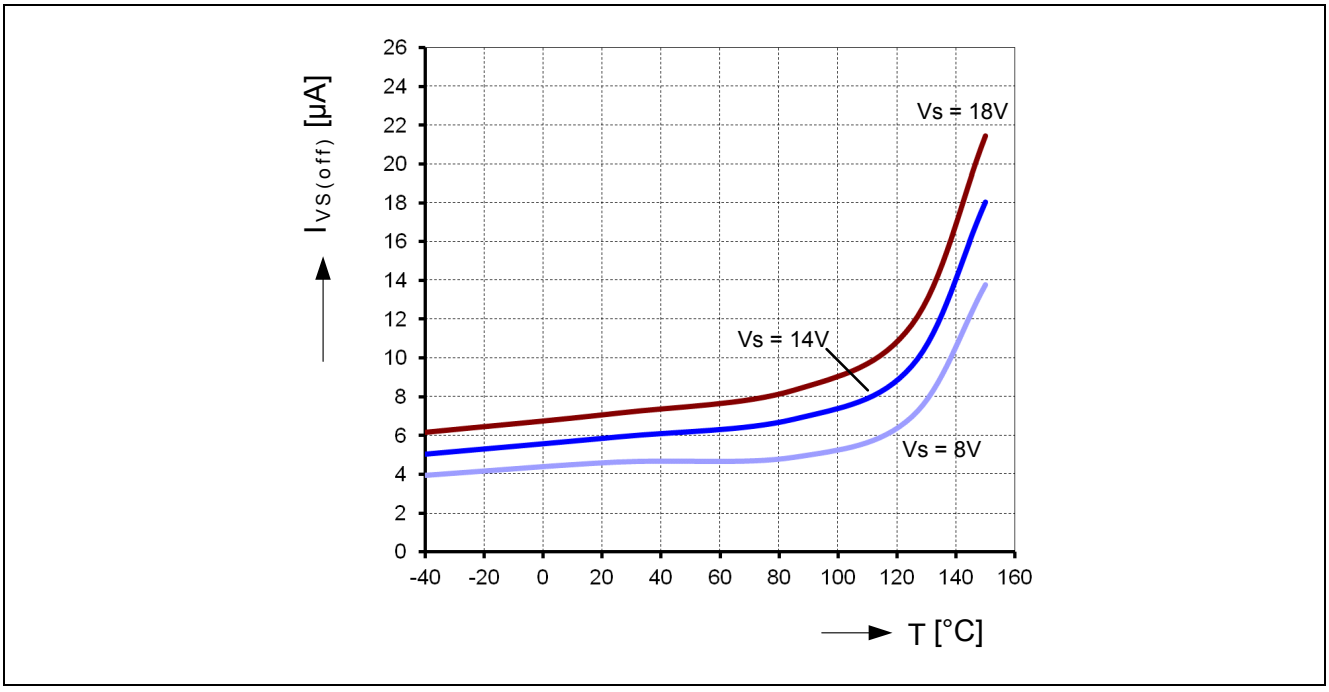


Figure 5 Typical Quiescent Current vs. Junction Temperature

5.2 Power Stages

The power stages of the BTN8962TA consist of a p-channel vertical DMOS transistor for the high side switch and a n-channel vertical DMOS transistor for the low side switch. All protection and diagnostic functions are located in a separate top chip. Both switches allow active freewheeling and thus minimizing power dissipation during PWM control.

The on state resistance R_{ON} is dependent on the supply voltage V_S as well as on the junction temperature T_j. The typical on state resistance characteristics are shown in **Figure 6**.

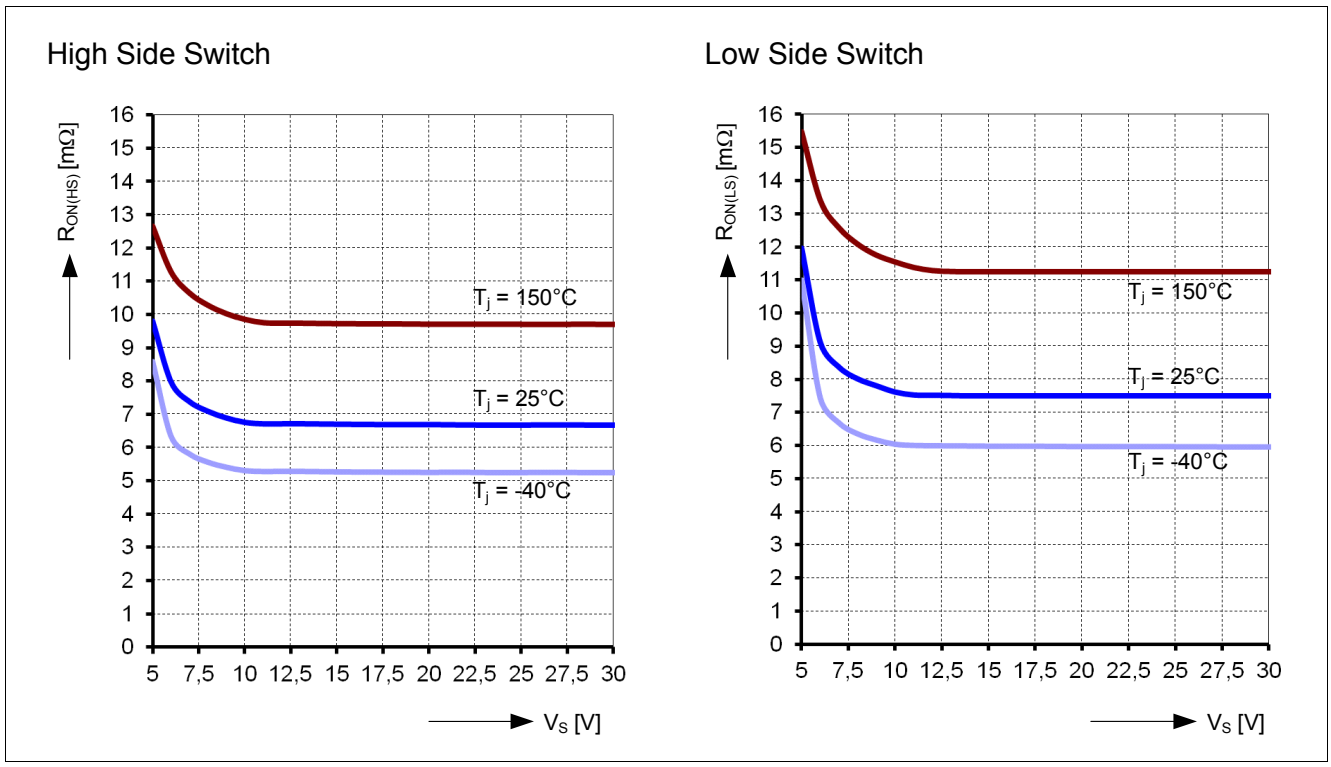


Figure 6 Typical ON State Resistance vs. Supply Voltage

5.2.1 Power Stages - Static Characteristics

V_S = 8 V to 18 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
High Side Switch - Static Characteristics							
5.2.1	ON State High Side Resistance	$R_{ON(HS)}$	–	6.7	–	mΩ	I_{OUT} = 9 A; V_S = 13.5 V; T_j = 25 °C; 1)
			–	10	13.4		T_j = 150 °C
			–	9	–	mΩ	I_{OUT} = 6 A; V_S = 6 V; T_j = 25 °C; 1)
			–	12	18.4		T_j = 150 °C
5.2.2	Leakage Current High Side	$I_{L(LKHS)}$	–	–	2	µA	V_{INH} = 0 V; V_{OUT} = 0 V; T_j < 85 °C; 1)
			–	–	50	µA	V_{INH} = 0 V; V_{OUT} = 0 V; T_j = 150 °C
5.2.3	Reverse Diode Forward-Voltage High Side[2)]	$V_{DS(HS)}$	–	0.9	–	V	I_{OUT} = -9 A; T_j = -40 °C; 1)
			–	0.8	–		T_j = 25 °C; 1)
			–	0.6	0.8		T_j = 150 °C
Low Side Switch - Static Characteristics							
5.2.4	ON State Low Side Resistance	$R_{ON(LS)}$	–	7.5	–	mΩ	I_{OUT} = -9 A; V_S = 13.5 V; T_j = 25 °C; 1)
			–	12	16.9		T_j = 150 °C
			–	10.5	–	mΩ	I_{OUT} = -6 A; V_S = 6 V; T_j = 25 °C; 1)
			–	15	23.8		T_j = 150 °C
5.2.5	Leakage Current Low Side	$I_{L(LKLS)}$	–	–	2	µA	V_{INH} = 0 V; V_{OUT} = V_S; T_j < 85 °C; 1)
			–	–	20	µA	V_{INH} = 0 V; V_{OUT} = V_S; T_j = 150 °C
5.2.6	Reverse Diode Forward-Voltage Low Side[2)]	$-V_{DS(LS)}$	–	0.9	–	V	I_{OUT} = 9 A; T_j = -40 °C; 1)
			–	0.8	–		T_j = 25 °C; 1)
			–	0.7	0.9		T_j = 150 °C

1) Not subject to production test, specified by design

2) Due to active freewheeling, diode is conducting only for a few µs, depending on R_{SR}

5.2.2 Switching Times

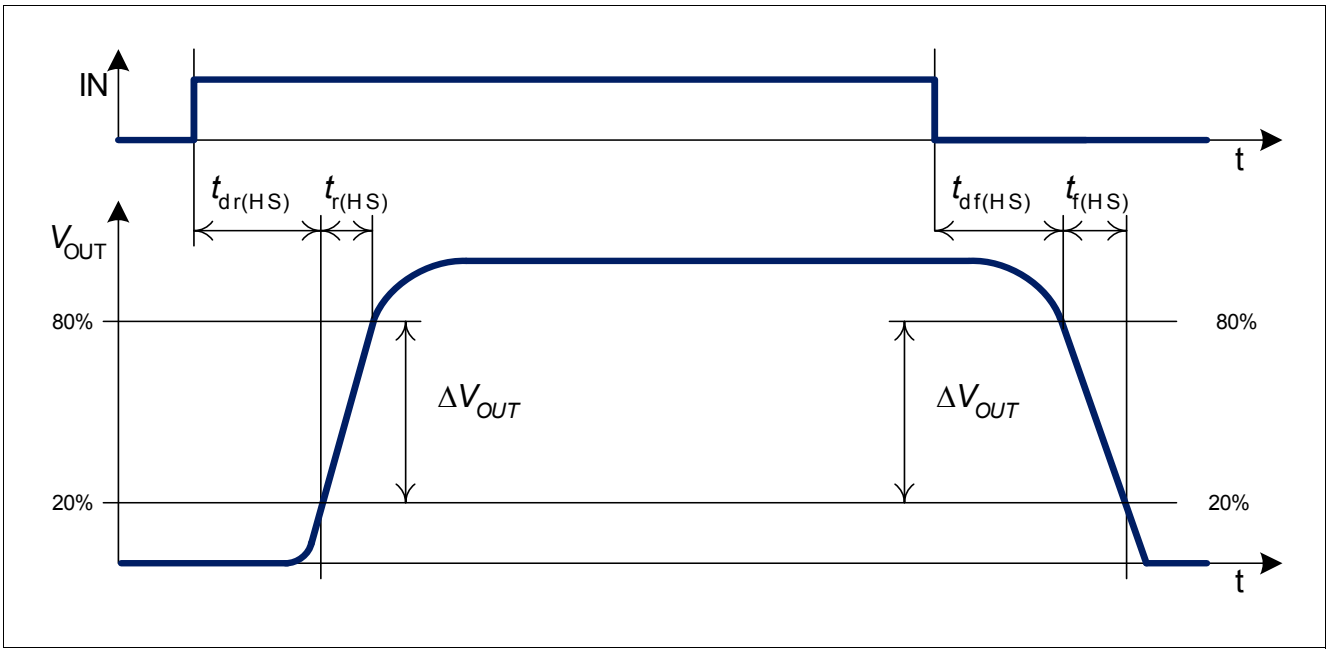


Figure 7 Definition of switching times high side (R_{load} to GND)

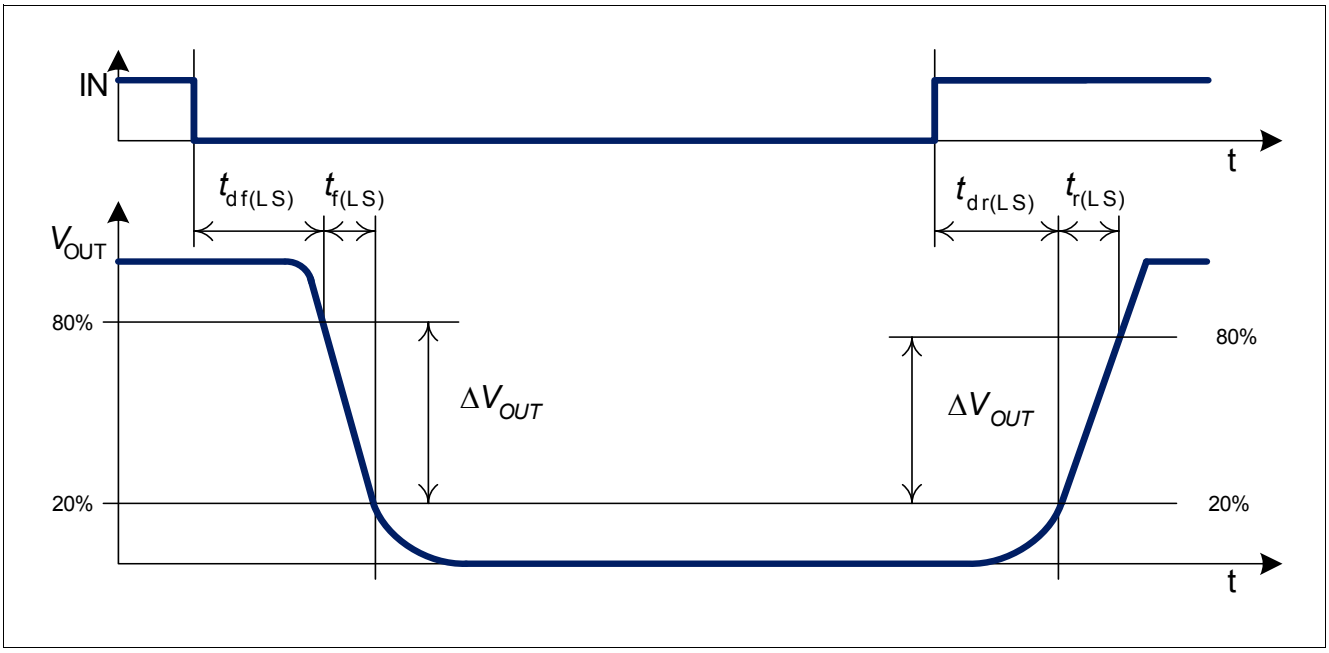


Figure 8 Definition of switching times low side (R_{load} to VS)

Due to the timing differences for the rising and the falling edge there will be a slight difference between the length of the input pulse and the length of the output pulse. It can be calculated using the following formulas:

- $\Delta t_{HS} = (t_{dr(HS)} + 0.5\ t_{r(HS)}) - (t_{df(HS)} + 0.5\ t_{f(HS)})$
- $\Delta t_{LS} = (t_{df(LS)} + 0.5\ t_{f(LS)}) - (t_{dr(LS)} + 0.5\ t_{r(LS)})$.

5.2.3 Power Stages - Dynamic Characteristics

V_S = 13.5 V, T_j = -40 °C to +150 °C, R_{load} = 2 Ω, 30µH < L_{load} < 40µH (in series to R_{load}), single pulse, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
High Side Switch Dynamic Characteristics							
5.2.7	Rise-Time of HS	$t_{r(HS)}$	0.05 – 0.2	0.25 0.35 1	0.8 – 5.6	µs	R_{SR} = 0 Ω R_{SR} = 5.1 kΩ R_{SR} = 51 kΩ
5.2.8	Switch ON Delay Time HS	$t_{dr(HS)}$	1.5 – 1.9	3.1 4.7 12.3	4.8 – 26.5	µs	R_{SR} = 0 Ω R_{SR} = 5.1 kΩ R_{SR} = 51 kΩ
5.2.9	Fall-Time of HS	$t_{f(HS)}$	0.05 – 0.2	0.25 0.35 1	0.8 – 5.6	µs	R_{SR} = 0 Ω R_{SR} = 5.1 kΩ R_{SR} = 51 kΩ
5.2.10	Switch OFF Delay Time HS	$t_{df(HS)}$	0.4 – 1.2	2.2 3.2 7.6	3.7 – 20	µs	R_{SR} = 0 Ω R_{SR} = 5.1 kΩ R_{SR} = 51 kΩ
Low Side Switch Dynamic Characteristics							
5.2.11	Rise-Time of LS	$t_{r(LS)}$	0.05 – 0.2	0.25 0.35 1	0.8 – 5.6	µs	R_{SR} = 0 Ω R_{SR} = 5.1 kΩ R_{SR} = 51 kΩ
5.2.12	Switch OFF Delay Time LS	$t_{dr(LS)}$	0.1 – 0.5	1.4 2 6	2.4 – 14	µs	R_{SR} = 0 Ω R_{SR} = 5.1 kΩ R_{SR} = 51 kΩ
5.2.13	Fall-Time of LS	$t_{f(LS)}$	0.05 – 0.2	0.25 0.35 1	0.8 – 5.6	µs	R_{SR} = 0 Ω R_{SR} = 5.1 kΩ R_{SR} = 51 kΩ
5.2.14	Switch ON Delay Time LS	$t_{df(LS)}$	1.4 – 2.3	3.7 5.5 14	5.6 – 31	µs	R_{SR} = 0 Ω R_{SR} = 5.1 kΩ R_{SR} = 51 kΩ

5.3 Protection Functions

The device provides integrated protection functions. These are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not to be used for continuous or repetitive operation, with the exception of the current limitation (**Chapter 5.3.3**). In case of overtemperature the BTN8962TA will apply the slew rate determined by the connected slew rate resistor. In current limitation mode the highest slew rate possible will be applied independent of the connected slew rate resistor. Overtemperature and overcurrent are indicated by a fault current $I_{IS(LIM)}$ at the IS pin as described in the paragraph **“Status Flag Diagnosis with Current Sense Capability” on Page 17** and **Figure 12**.

5.3.1 Undervoltage Shut Down

To avoid uncontrolled motion of the driven motor at low voltages the device shuts off (output is tri-state), if the supply voltage drops below the switch-off voltage $V_{UV(OFF)}$. The IC becomes active again with a hysteresis $V_{UV(HY)}$ if the supply voltage rises above the switch-on voltage $V_{UV(ON)}$.

5.3.2 Overtemperature Protection

The BTN8962TA is protected against overtemperature by an integrated temperature sensor. Overtemperature leads to a shut down of both output stages. This state is latched until the device is reset by a low signal with a minimum length of t_{reset} at the INH pin, provided that its temperature has decreased at least the thermal hysteresis ΔT in the meantime.

Repetitive use of the overtemperature protection impacts lifetime.

5.3.3 Current Limitation

The current in the bridge is measured in both switches. As soon as the current in forward direction in one switch (high side or low side) is reaching the limit I_{CLx}, this switch is deactivated and the other switch is activated for t_{CLS}. During that time all changes at the IN pin are ignored. However, the INH pin can still be used to switch both MOSFETs off. After t_{CLS} the switches return to their initial setting. The error signal at the IS pin is reset after 2 * t_{CLS}. Unintentional triggering of the current limitation by short current spikes (e.g. inflicted by EMI coming from the motor) is suppressed by internal filter circuitry. Due to thresholds and reaction delay times of the filter circuitry the effective current limitation level I_{CLx} depends on the slew rate of the load current dI/dt as shown in **Figure 10**.

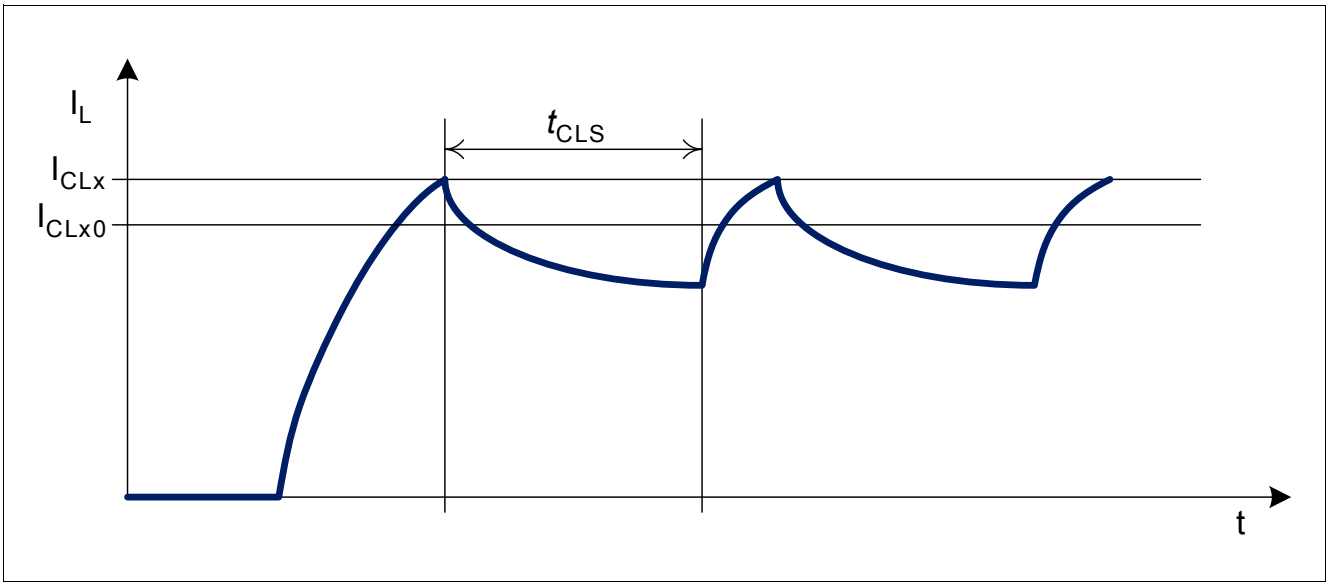


Figure 9 Timing Diagram Current Limitation (Inductive Load)

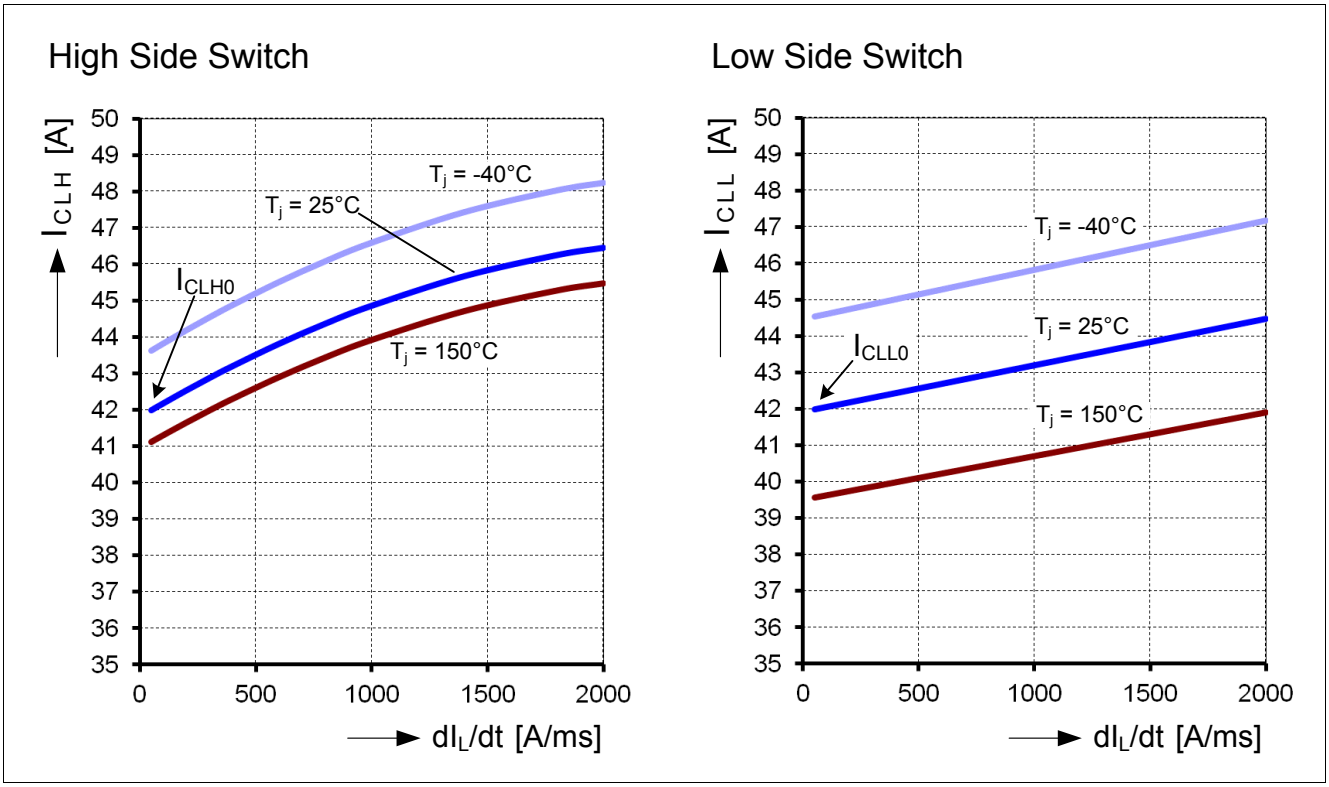


Figure 10 Typical Current Limitation Detection Level vs. Current Slew Rate dI_L/dt

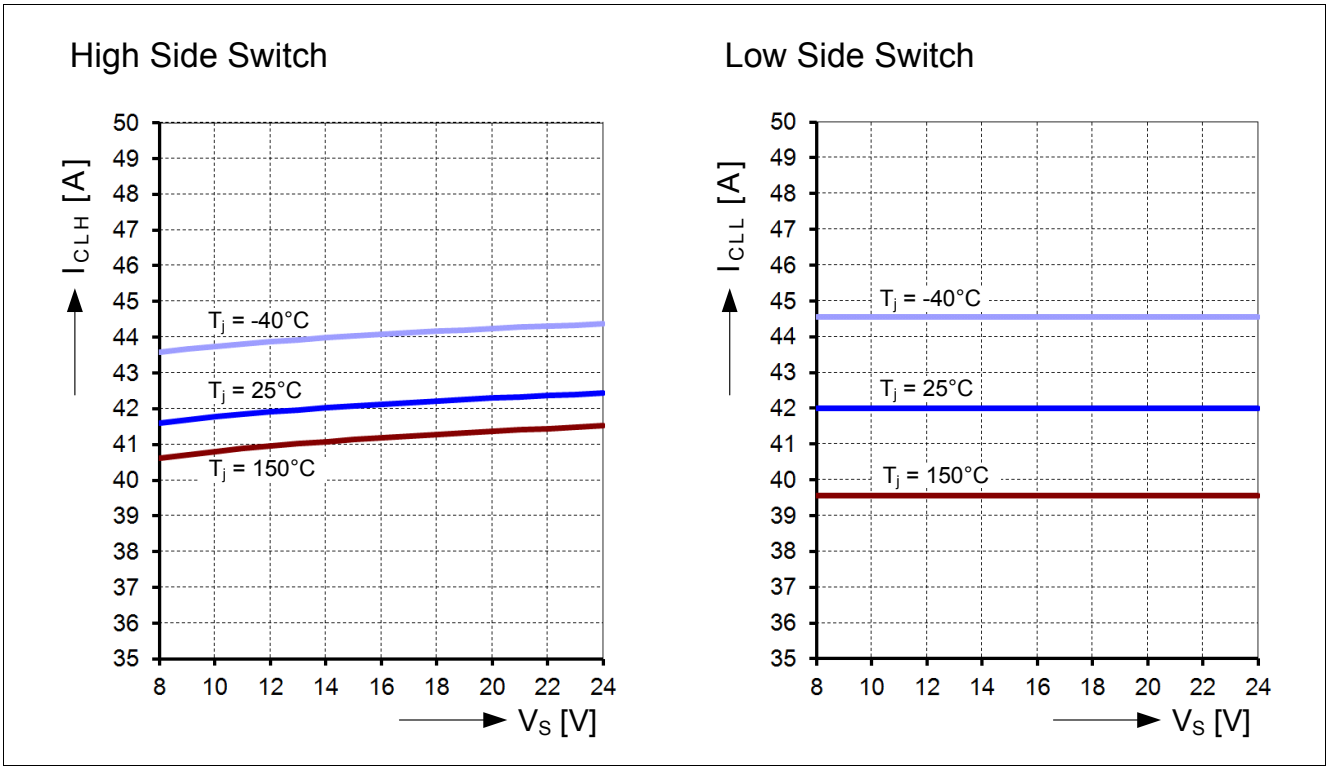


Figure 11 Typical Current Limitation Detection Levels vs. Supply Voltage

In combination with a typical inductive load, such as a motor, this results in a switched mode current limitation. This method of limiting the current has the advantage of greatly reduced power dissipation in the BTN8962TA

compared to driving the MOSFET in linear mode. Therefore it is possible to use the current limitation for a short time without exceeding the maximum allowed junction temperature (e.g. for limiting the inrush current during motor start up). However, the regular use of the current limitation is allowed as long as the specified maximum junction temperature is not exceeded. Exceeding this temperature can reduce the lifetime of the device.

5.3.4 Short Circuit Protection

The device provides embedded protection functions against

- output short circuit to ground
- output short circuit to supply voltage
- short circuit of load

The short circuit protection is realized by the previously described current limitation in combination with the over-temperature shut down of the device.

5.3.5 Electrical Characteristics - Protection Functions

V_S = 8 V to 18 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Under Voltage Shut Down							
5.3.1	Switch-ON Voltage	$V_{UV(ON)}$	–	–	5.5	V	V_S increasing
5.3.2	Switch-OFF Voltage[1)]	$V_{UV(OFF)}$	3.0	–	4.5	V	V_S decreasing, INH = 1
5.3.3	ON/OFF Hysteresis	$V_{UV(HY)}$	–	0.2	–	V	[2)]
Current Limitation							
5.3.4	Current Limitation Detection level High Side	I_{CLH0}	30	42	54	A	V_S = 13.5 V
5.3.5	Current Limitation Detection level Low Side	I_{CLL0}	30	42	54	A	V_S = 13.5 V
Current Limitation Timing							
5.3.6	Shut OFF Time for HS and LS	t_{CLS}	70	115	210	µs	V_S = 13.5 V; [2)]
Thermal Shut Down							
5.3.7	Thermal Shut Down Junction Temperature	T_{jSD}	155	175	200	°C	–
5.3.8	Thermal Switch ON Junction Temperature	T_{jSO}	150	–	190	°C	–
5.3.9	Thermal Hysteresis	ΔT	–	7	–	K	[2)]
5.3.10	Reset Pulse at INH Pin (INH low)	t_{reset}	4	–	–	µs	[2)]

1) With decreasing V_s < 5.5V activation of the Current Limitation mode may occur before Undervoltage Shut Down.

2) Not subject to production test, specified by design.

5.4 Control and Diagnostics

5.4.1 Input Circuit

The control inputs IN and INH consist of TTL/CMOS compatible schmitt triggers with hysteresis which control the integrated gate drivers for the MOSFETs. Setting the INH pin to high enables the device. In this condition one of the two power switches is switched on depending on the status of the IN pin. To deactivate both switches, the INH pin has to be set to low. No external driver is needed. The BTN8962TA can be interfaced directly to a microcontroller, as long as the maximum ratings in **Chapter 4.1** are not exceeded.

5.4.2 Dead Time Generation

In bridge applications it has to be assured that the highside and lowside MOSFET are not conducting at the same time, connecting directly the battery voltage to GND. This is assured by a circuit in the driver IC, generating a so called dead time between switching off one MOSFET and switching on the other. The dead time generated in the driver IC is automatically adjusted to the selected slew rate.

5.4.3 Adjustable Slew Rate

In order to optimize electromagnetic emission, the switching speed of the MOSFETs is adjustable by an external resistor. The slew rate pin SR allows the user to optimize the balance between emission and power dissipation within his own application by connecting an external resistor R_{SR} to GND.

5.4.4 Status Flag Diagnosis with Current Sense Capability

The sense pin IS is used as a combined current sense and error flag output.

In normal operation (current sense mode), a current source is connected to the status pin, which delivers a current proportional to the forward load current flowing through the active high side switch. The sense current can be calculated out of the load current by the following equation:

$$I_{IS} = \frac{1}{dk_{ILIS}} \cdot I_L + I_{IS(offset)} \quad (1)$$

The other way around, the load current can be calculated out of the sense current by following equation:

$$I_L = dk_{ILIS} \cdot (I_{IS} - I_{IS(offset)}) \quad (2)$$

The differential current sense ratio dk_{ilis} is defined by:

$$dk_{ILIS} = \frac{I_{L2} - I_{L1}}{I_{IS}(I_{L2}) - I_{IS}(I_{L1})} \quad (3)$$

If the high side drain current is zero ($I_{SD(HS)}$ = 0A) the offset current $I_{IS} = I_{IS(offset)}$ still will be driven.

The external resistor R_{IS} determines the voltage per IS output current. The voltage can be calculated by $V_{IS} = R_{IS} \cdot I_{IS}$.

In case of a fault condition the status output is connected to a current source which is independent of the load current and provides $I_{IS(lim)}$. The maximum voltage at the IS pin is determined by the choice of the external resistor and the supply voltage. In case of current limitation the $I_{IS(lim)}$ is activated for 2 * t_{CLS}.

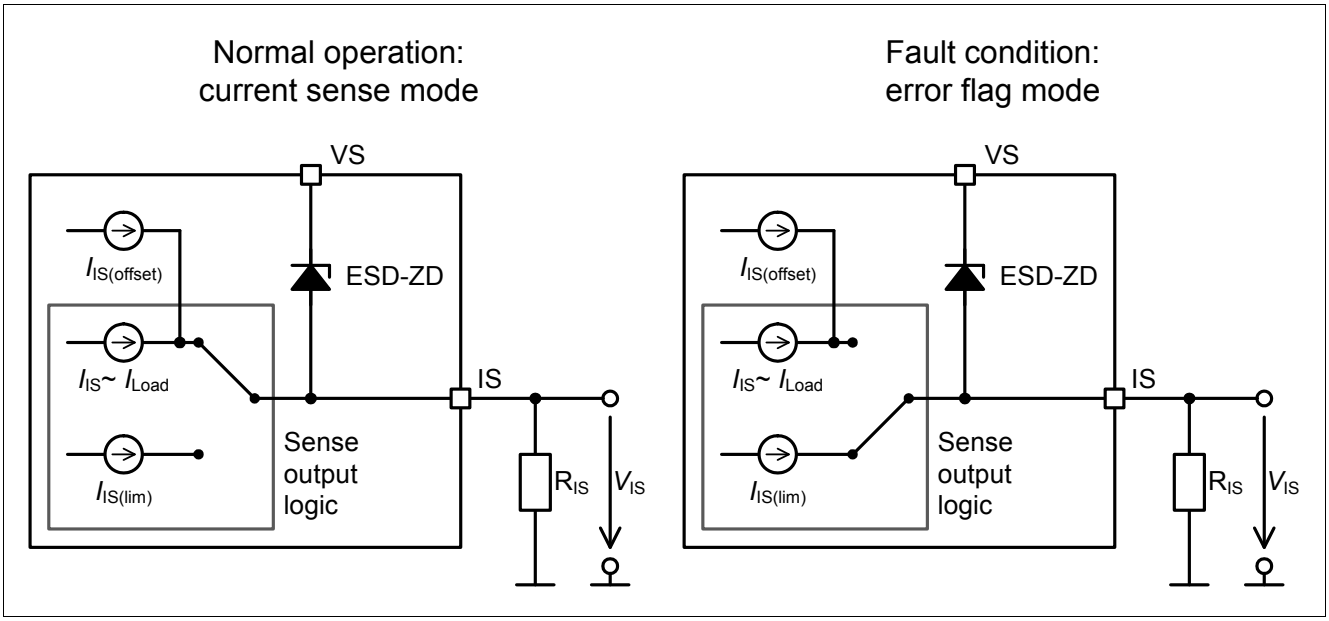


Figure 12 Sense Current and Fault Current

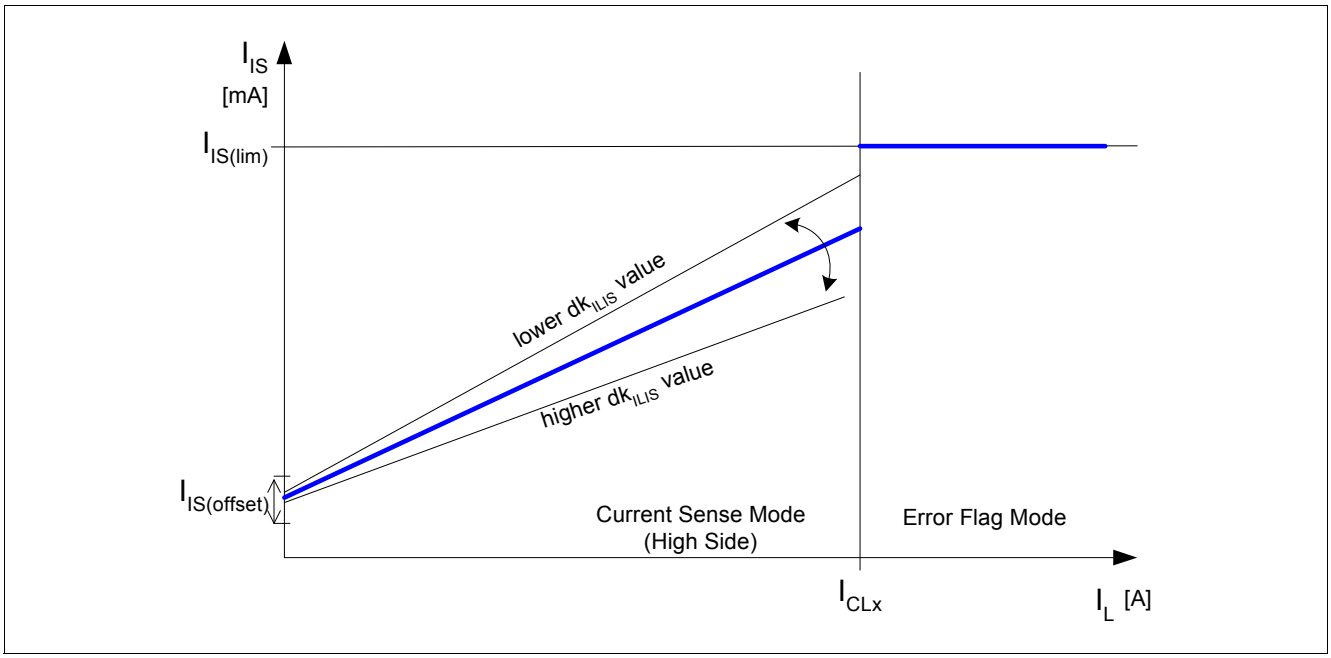


Figure 13 Sense Current vs. Load Current

5.4.5 Truth Table

Device State	Inputs		Outputs			Mode
	INH	IN	HSS	LSS	IS	
Normal Operation	0	X	OFF	OFF	0	Stand-by mode
	1	0	OFF	ON	$I_{IS(offset)}$	LSS active
	1	1	ON	OFF	CS	HSS active
Under-Voltage (UV)	X	X	OFF	OFF	0	UV lockout, reset
Overtemperature (OT) or Short Circuit of HSS or LSS	0	X	OFF	OFF	0	Stand-by mode, reset of latch
	1	X	OFF	OFF	1	Shut-down with latch, error detected
Current Limitation Mode/ Overcurrent (OC)	1	1	OFF	ON	1	Switched mode, error detected[1)]
	1	0	ON	OFF	1	Switched mode, error detected[1)]

1) Will return to normal operation after t_{CLS}; Error signal is reset after 2*t_{CLS} (see **Chapter 5.3.3**)

Inputs	Switches	Current Sense / Status Flag IS
0 = Logic LOW	OFF = switched off	$I_{IS(offset)}$ = Current sense - Offset (for conditions see table: **Current Sense**)
1 = Logic HIGH	ON = switched on	CS = Current sense - high side (for conditions see table: **Current Sense**)
X = 0 or 1		1 = Logic HIGH (error)

5.4.6 Electrical Characteristics - Control and Diagnostics

V_S = 8 V to 18 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Control Inputs (IN and INH)							
5.4.1	High level Voltage INH, IN	$V_{INH(H)}$ $V_{IN(H)}$	– –	1.75 1.6	2.15 2	V	–
5.4.2	Low level Voltage INH, IN	$V_{INH(L)}$ $V_{IN(L)}$	1.1	1.4	–	V	–
5.4.3	Input Voltage hysteresis	V_{INHHY} V_{INHY}	– –	350 200	– –	mV	1)
5.4.4	Input Current high level	$I_{INH(H)}$ $I_{IN(H)}$	10	30	150	µA	V_{IN} = V_{INH} = 5.3 V
5.4.5	Input Current low level	$I_{INH(L)}$ $I_{IN(L)}$	10	25	125	µA	V_{IN} = V_{INH} = 0.4 V
Current Sense							
5.4.6	Differential Current Sense ratio in static on-condition dk_{ILIS} = dI_L / dI_{IS}	dk_{ILIS}	7.2	10	12.8	10^3	R_{IS} = 1 kΩ I_{L1} = 3 A I_{L2} = 15 A
5.4.7	Maximum analog Sense Current, Sense Current in fault Condition	$I_{IS(lim)}$	4	5	6.5	mA	V_S = 13.5 V R_{IS} = 1kΩ
5.4.8	Isense Leakage current	I_{ISL}	–	–	1	µA	V_{INH} = 0 V
5.4.9	Isense offset current	$I_{IS(offset)}$	50	200	440	µA	V_S = 18V; V_{INH} = 5 V $I_{SD(HS)}$ = 0 A

1) Not subject to production test, specified by design

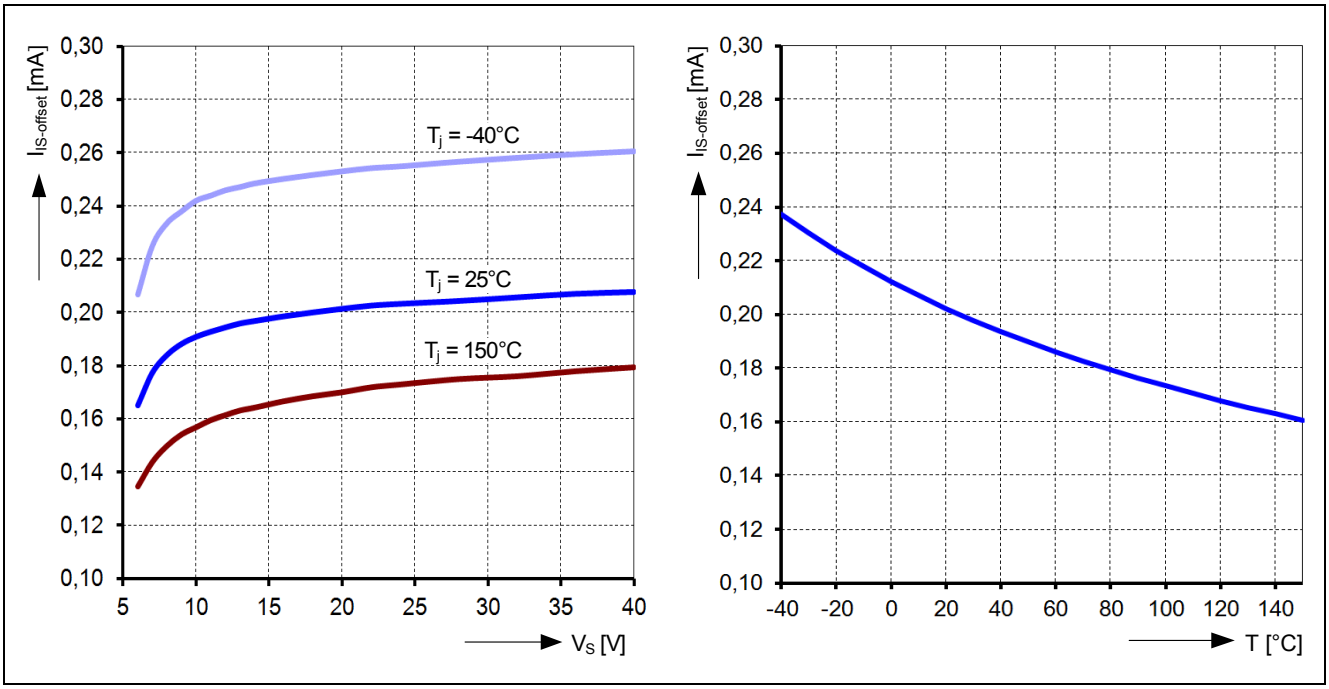


Figure 14 Typical Current Sense Offset Current

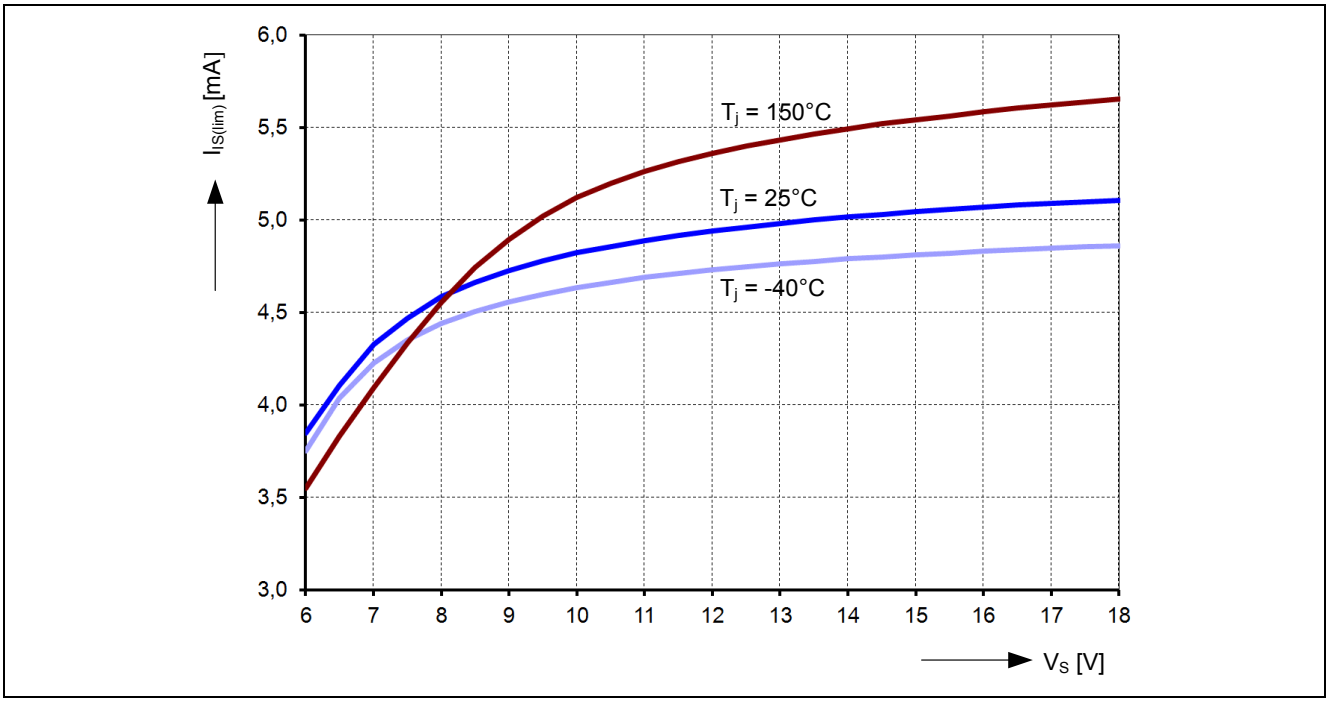


Figure 15 Typical characteristic of the maximum analog Sense Current in fault condition (Pos. 5.4.7.)

6 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

6.1 Application Circuit

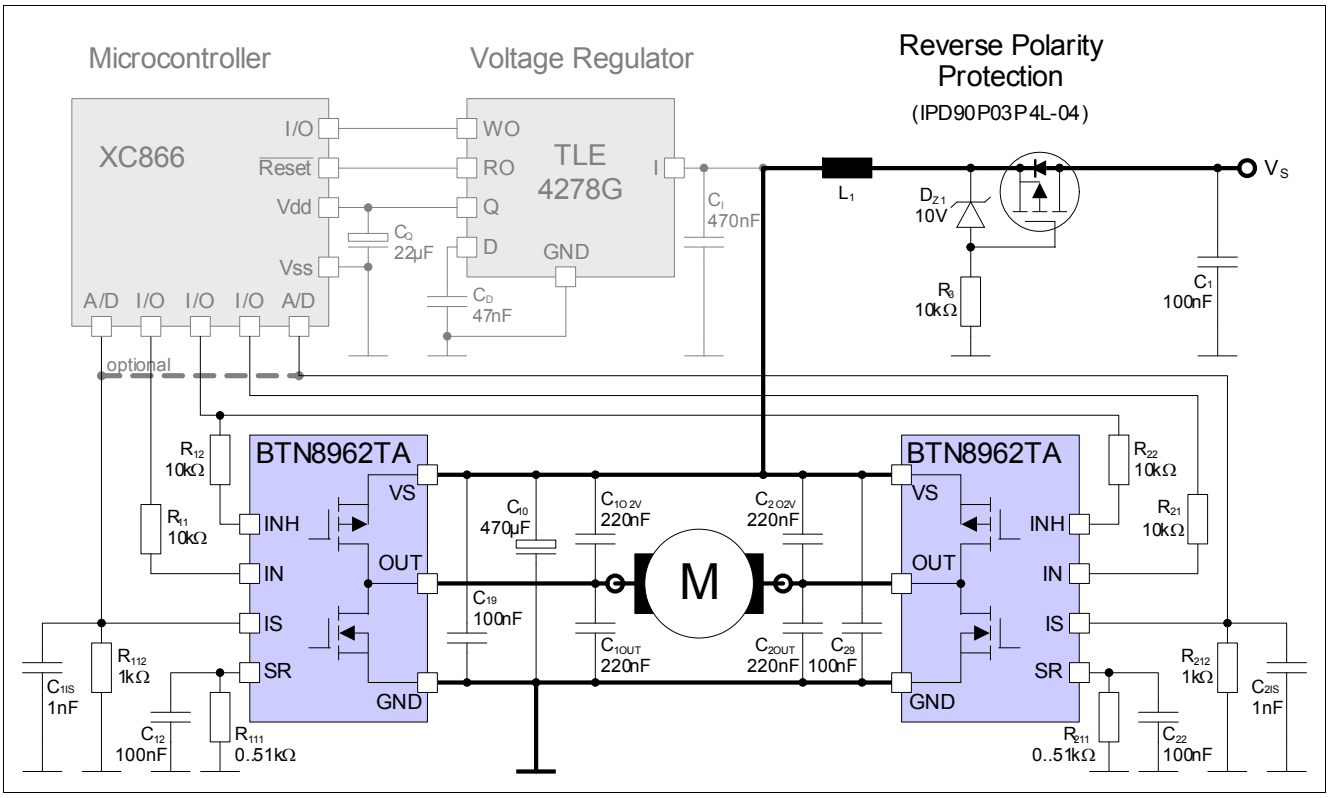


Figure 16 Application Circuit: H-Bridge with two BTN8962TA

Note: This is a simplified example of an application circuit. The function must be verified in the real application.

6.2 Layout Considerations

Due to the fast switching times for high currents, special care has to be taken to the PCB layout. Stray inductances have to be minimized in the power bridge design as it is necessary in all switched high power bridges. The BTN8962TA has no separate pin for power ground and logic ground. Therefore it is recommended to assure that the offset between the ground connection of the slew rate resistor, the current sense resistor and ground pin of the device (GND / pin 1) is minimized. If the BTN8962TA is used in a H-bridge or B6 bridge design, the voltage offset between the GND pins of the different devices should be small as well.

Due to the fast switching behavior of the device in current limitation mode a low ESR electrolytic capacitor C_{10} from VS to GND is necessary. This prevents destructive voltage peaks and drops on VS. This is needed for both PWM and non PWM controlled applications. To assure efficiency of C_{10} and C_{19}/ C_{29} the stray inductance must be low. Therefore the capacitors must be placed very close to the device pins. The value of the capacitors must be verified in the real application, taking care for low ripple and transients at the Vs pin of the BTN8962TA.

The digital inputs need to be protected from excess currents (e.g. caused by induced voltage spikes) by series resistors greater than 7kΩ.

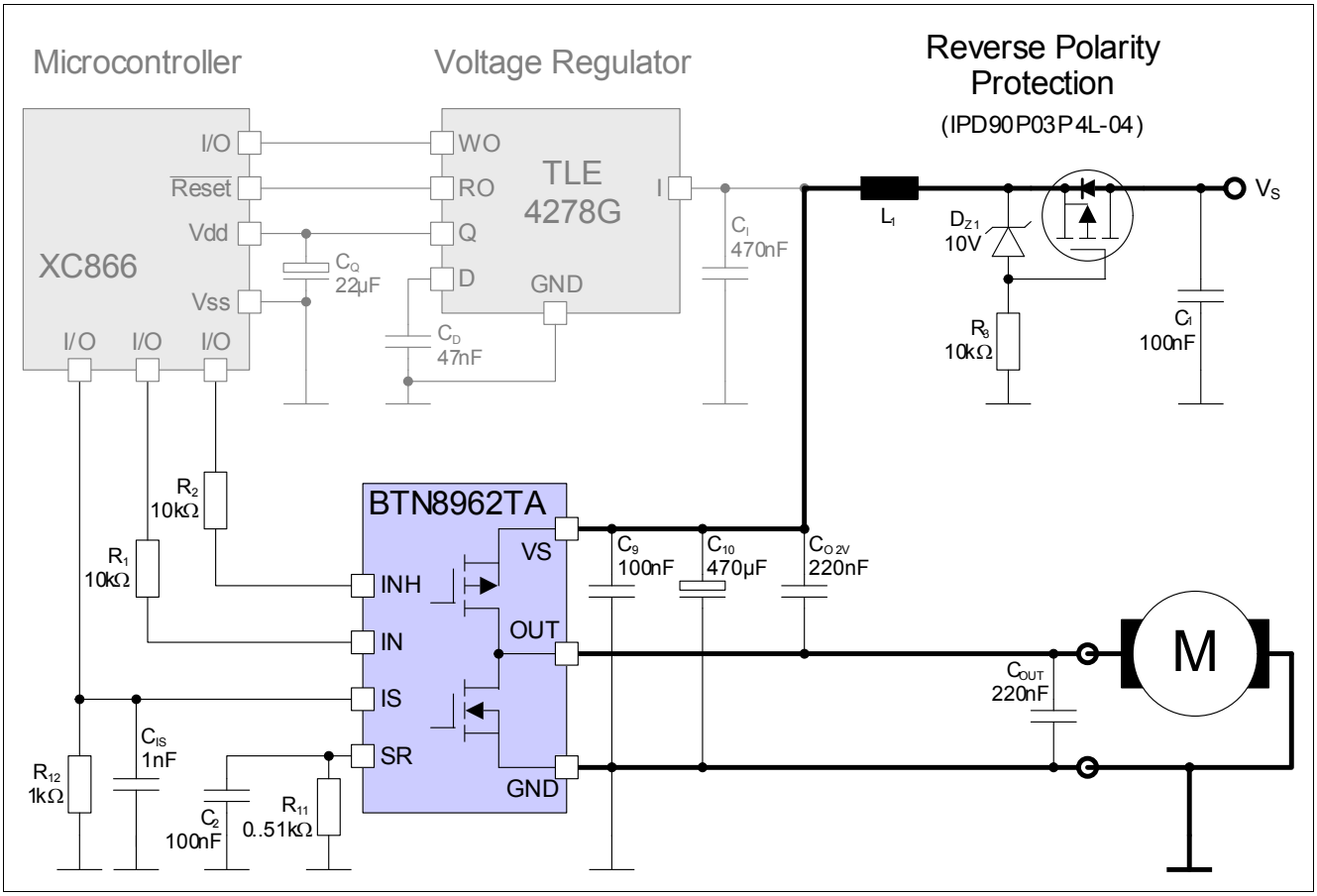


Figure 17 Application Circuit: Half-Bridge with a BTN8962TA (Load to GND)

Note: This is a simplified example of an application circuit. The function must be verified in the real application.

6.3 PWM Control

For the selection of the max. PWM frequency the choosen rise/fall-time and the requirements on the duty cycle have to be taken into account. We recommend a PWM-period at least 10 times the rise-time.

Example:

Rise-time = fall-time = 4µs.

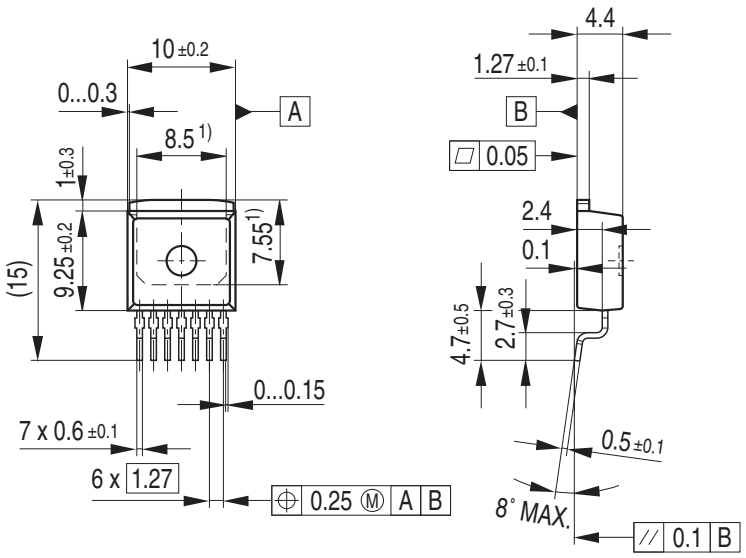
=> T-PWM = 10 * 4µs = 40µs.

=> f-PWM = 25kHz.

The min. and max. value of the duty cycle (PWM ON to OFF percentage) is determined by the real fall time plus the real rise time. In this example a duty cycle make sense from approximately 20% to 80%.

If a wider duty cycle range is needed, the PWM frequency could be decreased and/or the rise/fall-time could be accelerated.

7 Package Outlines



1) Typical
Metal surface min. X = 7.25, Y = 6.9
All metal surfaces tin plated, except area of cut.

GPT09114

Footprint

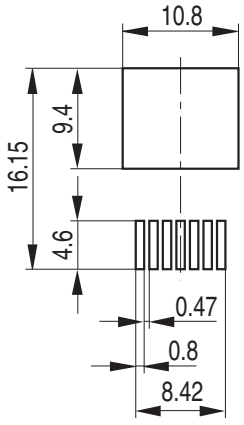


Figure 18 PG-TO263-7-1 (Plastic Green Transistor Single Outline Package)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

8 Revision History

Initial release.

Edition 2013-05-17

Published by
Infineon Technologies AG
81726 Munich, Germany

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